

PRODUCT SPECIFICATION

6252B5-PRB

Wi-Fi Dual-band 2x2 11ax + Bluetooth 5.2

Combo Module

Version:v1.1



6252B5-PRB Module Datasheet

Ordering Information	Part NO.	Description
	FG6252B5PR-00	RTL8852BE-VR-CG, a/b/g/n/ac/ax Wi-Fi, 2T2R, BT5.2, 13*15mm, PCIE,UART (PIN WIFI5 8822BE)

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

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1. General Description

1.1 Introduction

The 6252B5-PRB is a highly integrated single-chip that support 2-stream 802.11ax solutions with Multi-user MIMO (Multiple-Input, Multiple-Output) with Wireless LAN (WLAN) PCI Express network interface controller and HS-UART mixed interface . It combines a WLAN MAC, a 2T2R capable WLAN baseband, and RF in a single chip. The 6252B5-PRB provides a complete solution for a high-performance integrated wireless and Bluetooth device.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

1.2 Description

Model Name	6252B5-PRB
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 13 x 15 x2.37 mm
Wi-Fi Interface	Support PCIE
BT Interface	UART
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	0°C to 70°C
Storage temperature	-40°C to 125°C

2. Features

General Features

- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac/ax compatible WLAN
- Support 2.4Ghz and 5Ghz band channels
- Maximum PHY data rate up to 286.8 Mbps using 20MHz bandwidth, 573.5Mbps using 40MHz bandwidth, and 1201Mbps using 80MHz bandwidth
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n/ac devices while operating at 802.11ax data rates
- IEEE 802.11a/b/g/n/ac/ax compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2, WPA3). Open, shared key, and pair-wise key authentication services
- 20MHz / 40MHz / 80MHz bandwidth transmission

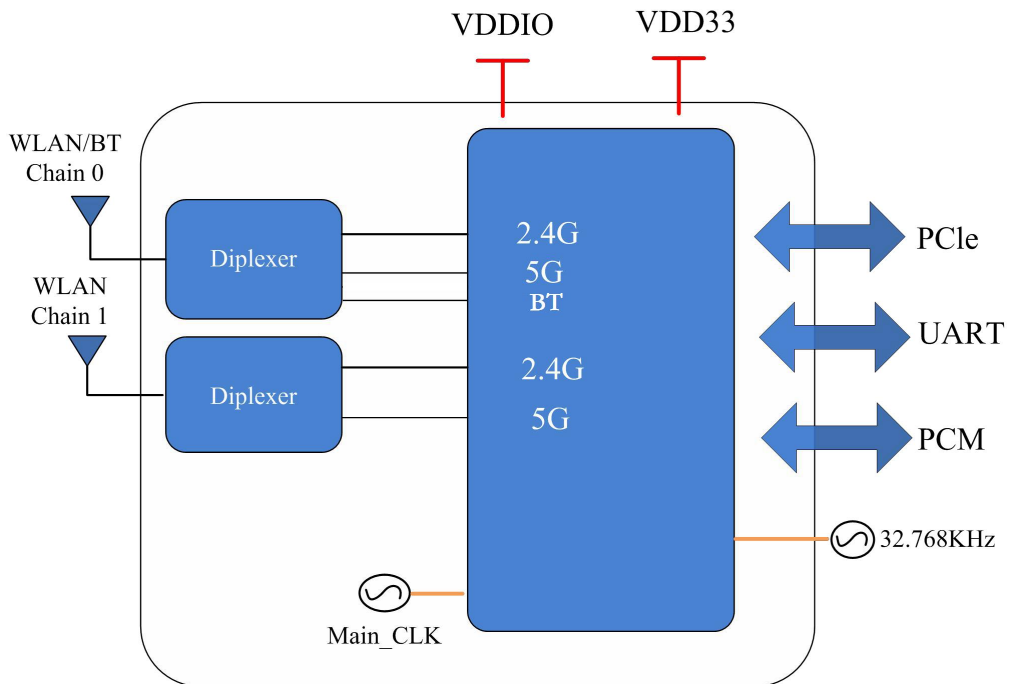
WLAN Interface

- PCIe LTR/L1.Off state supported.

Bluetooth Features

- Complies with HS-UART with configurable baud rate for Bluetooth
- Support Bluetooth 5 system (BT 5.2 Logo Compliant)
- Compatible with Bluetooth v2.1+EDR
- Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states

3. Block Diagram



4. General Specification

4.1 2.4GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n/ac/ax Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz: Ch1 ~ Ch14	
Test Items	Typical Value	EVM
Output Power	802.11b /11Mbps : 19dBm ± 2 dB	EVM ≤ -9dB
	802.11g /54Mbps : 18dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 17dBm ± 2 dB	EVM ≤ -28dB
	802.11ac VHT20 MCS8: 16dBm ± 2 dB	EVM ≤ -30dB
	802.11ac VHT40 MCS9: 15dBm ± 2 dB	EVM ≤ -32dB
	802.11ax HE20 MCS11: 13dBm ± 2 dB	EVM ≤ -35dB
	802.11ax HE40 MCS11: 13dBm ± 2 dB	EVM ≤ -35dB
Spectrum Mask	Meet with IEEE standard	

Freq. Tolerance	± 20ppm		
Test Items	TYP Test Value		Standard Value
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps	PER @ -91 dBm	≤-83 dBm
	- 11Mbps	PER @ -84 dBm	≤-76 dBm
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps	PER @ -87 dBm	≤-85 dBm
	- 54Mbps	PER @ -70 dBm	≤-68 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -87 dBm	≤-85 dBm
	- MCS=7	PER @ -69 dBm	≤-67 dBm
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0,	PER @ -84 dBm	≤-82 dBm
	- MCS=7,	PER @ -66 dBm	≤-64 dBm
SISO Receive Sensitivity (11ac,20MHz) @10% PER	- MCS=0,	PER @ -90 dBm	≤ -82 dBm
	- MCS=8,	PER @ -64 dBm	≤ -60 dBm
SISO Receive Sensitivity (11ac ,40MHz) @10% PER	- MCS=0,	PER @ -87 dBm	≤ -79 dBm
	- MCS=9,	PER @ -59 dBm	≤ -55 dBm
SISO Receive Sensitivity (11ax,20MHz) @10% PER	- MCS=0,	PER @ -90 dBm	≤-74 dBm
	- MCS=11,	PER @ -60 dBm	≤-52 dBm
SISO Receive Sensitivity (11ax ,40MHz) @10% PER	- MCS=0,	PER @ -87 dBm	≤-71 dBm
	- MCS=11,	PER @ -57 dBm	≤-49 dBm
Maximum Input Level	802.11b : -10 dBm		
	802.11g/n : -20 dBm		
Antenna Reference	Small antennas with 0~2 dBi peak gain		

4.2 5GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11a/n/ac/ax , Wi-Fi compliant	
Frequency Range	4.900 GHz ~ 5.845 GHz (5.0 GHz ISM Band)	
Number of Channels	5.0GHz: Please see the table1	
Test Items	Typical Value	EVM
Output Power ²	802.11a /54Mbps: 18 dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7: 17 dBm ± 2 dB	EVM ≤ -28dB
	802.11ac VHT20 MCS8: 16 dBm ± 2 dB	EVM ≤ -30dB
	802.11ac VHT40 MCS9: 15 dBm ± 2 dB	EVM ≤ -32dB
	802.11ac VHT80 MCS9: 15 dBm ± 2 dB	EVM ≤ -32dB
	802.11ax HE20 MCS11: 13 dBm ± 2 dB	EVM ≤ -35dB
	802.11ax HE40 MCS11: 13 dBm ± 2 dB	EVM ≤ -35dB

	802.11ax HE80 MCS11: 13 dBm ± 2 dB	EVM ≤ -35dB
Test Items	Test Value	Standard Value
SISO Receive Sensitivity (11a,20MHz) @10% PER	- 6Mbps @ -90 dBm	≤-85 dBm
	- 54Mbps @ -71 dBm	≤-68 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 @ -90 dBm	≤-85 dBm
	- MCS=7 @ -69 dBm	≤-67 dBm
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 @ -87 dBm	≤-82 dBm
	- MCS=7 @ -66 dBm	≤-64 dBm
SISO Receive Sensitivity (11ac,20MHz)@10% PER	- MCS=0, NSS1 @ 90 dBm	≤-82 dBm
	- MCS=8, NSS1 @ -64 dBm	≤-60 dBm
SISO Receive Sensitivity (11ac,40MHz) @10% PER	- MCS=0, NSS1 @ -87 dBm	≤-79 dBm
	- MCS=9, NSS1 @ -59 dBm	≤-55 dBm
SISO Receive Sensitivity (11ac,80MHz) @10% PER	- MCS=0, NSS1 @ -84 dBm	≤-79 dBm
	- MCS=9, NSS1 @ -56 dBm	≤-54 dBm
SISO Receive Sensitivity (11ax,20MHz) @10% PER	- MCS=0 @ -90 dBm	≤-74 dBm
	- MCS=11 @ -60 dBm	≤-52 dBm
SISO Receive Sensitivity (11ax,40MHz) @10% PER	- MCS=0 @ -87 dBm	≤-71 dBm
	- MCS=11 @ -57 dBm	≤-49 dBm
SISO Receive Sensitivity (11ax,80MHz) @10% PER	- MCS=0 @ -84 dBm	≤-68 dBm
	- MCS=11 @ -54 dBm	≤-46 dBm
Maximum Input Level	802.11a/n: -30 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

15GHz(20MHz) Channel table

Band range	Operating Channel Numbers	Channel center frequencies(MHz)
5180MHz~5240MHz	36	5180
	40	5200
	44	5220
	48	5240
5260MHz~5320MHz	52	5260
	56	5280
	60	5300
	64	5320
5550MHz~5700MHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640

	132	5660
	136	5680
	140	5700
5745MHz~5825MHz	149	5745
	153	5765
	157	5785
	161	5805
	165	5825

4.3 Bluetooth Specification

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V5.2 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	GFSK, $\pi/4$ -DQPSK, 8-DPSK		
RF Specification			
	Min(dBm)	Typical(dBm)	Max(dBm)
Output Power (Class 1)	2	5	8
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-89	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)		-86	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-83	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

5. ID setting information

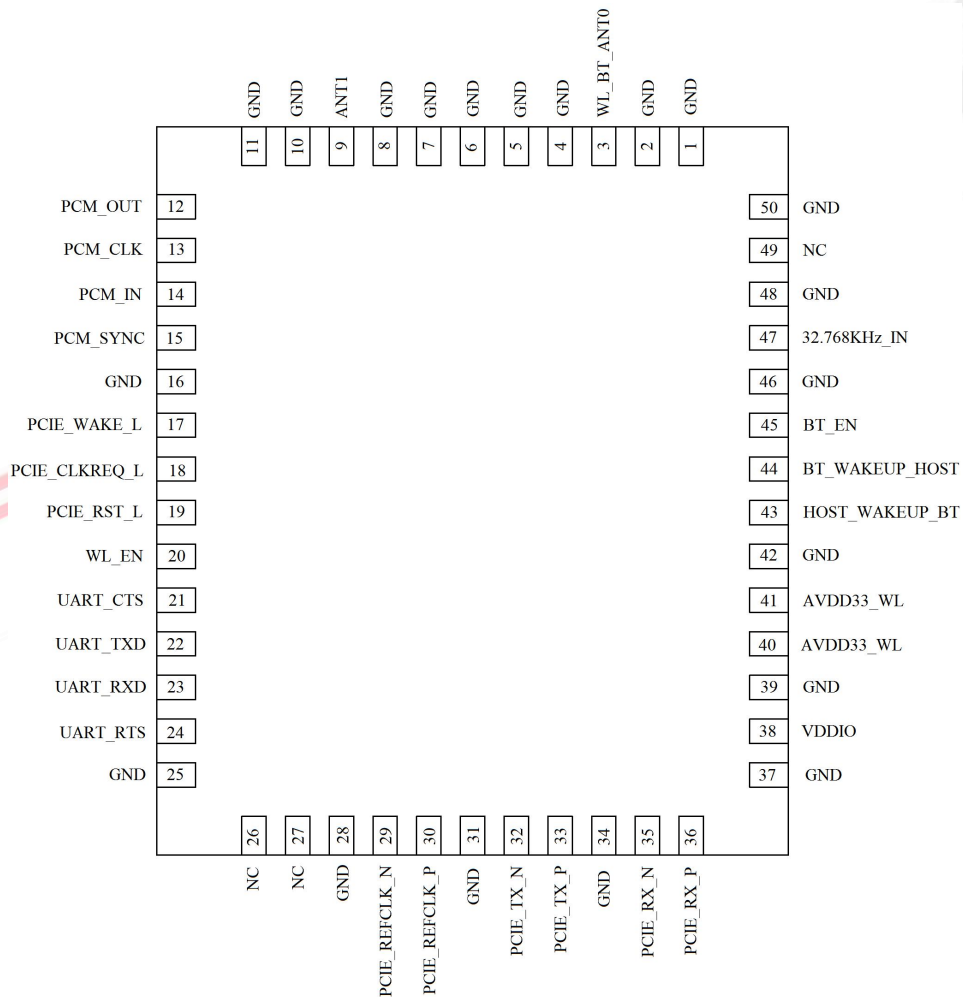
WI-FI

Vendor ID	-
Product ID	-

6. Pin Definition

6.1 Pin Outline

< TOP VIEW >



6.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1、 2	GND	—	Ground connections	
3	WL_BT_ANT0	I/O	WL_BT_ANT0 I/O	
4~8	GND	—	Ground connections	
9	ANT1	I/O	ANT1 RF I/O	
10、 11	GND	—	Ground connections	
12	PCM_OUT	O	PCM Data output	VDDIO
13	PCM_CLK	I/O	PCM clock	VDDIO
14	PCM_IN	I	PCM data input	VDDIO
15	PCM_SYNC	I/O	PCM sync signal	VDDIO
16	GND	—	Ground connections	
17	PCIE_WAKE_L	O	PCI-e wake up host, open drain, active low.	3.3V
18	PCIE_CLKREQ_L	I	PCI-e reference clock request signal, open drain, active low .	3.3V
19	PCIE_RST_L	I	PCI-e reset module, active low.	3.3V
20	WL_EN	I	WLAN enable signal, pull low to disable WL.	VDDIO
21	UART_CTS	I	Bluetooth UART interface	VDDIO
22	UART_TXD	O	Bluetooth UART interface	VDDIO
23	UART_RXD	I	Bluetooth UART interface	VDDIO
24	UART_RTS	O	Bluetooth UART interface (Module side is connect to GND)	
25	GND	—	Ground connections	
26	NC	—	No connection (Module side is BT_LOG)	
27	NC	—	No connection	
28	GND	—	Ground connections	
29	PCIE_REFCLK_N	I	PCI-E CLK Difference -	
30	PCIE_REFCLK_P	I	PCI-E CLK Difference +	
31	GND	—	Ground connections	
32	PCIE_TX_N	O	PCI-E Data Out Difference -	
33	PCIE_TX_P	O	PCI-E Data Out Difference +	
34	GND	—	Ground connections	

35	PCIE_RX_N	I	PCI-E Data IN Difference -	
36	PCIE_RX_P	I	PCI-E Data IN Difference +	
37	GND	—	Ground connections	
38	VDDIO	—	External power source input for IO domain	3.3V
39	GND	—	Ground connections	
40	AVDD33_WL	P	Main power source input	3.3V
41	AVDD33_WL	P	Main power source input	3.3V
42	GND	—	Ground connections	
43	HOST_WAKEUP_BT	I	Host wake up Bluetooth.	VDDIO
44	BT_WAKEUP_HOST	O	Bluetooth wake up host signal, module internal pull high.	VDDIO
45	BT_EN	I	Bluetooth enable signal, Pull low disable BT.	VDDIO
46	GND	—	Ground connections	
47	32.768KHz_IN	I	External sleep clock input(32.768kHz) .	
48	GND	—	Ground connections	
49	NC		No connection	
50	GND	—	Ground connections	

P:POWER I:INPUT O:OUTPUT VDDIO:3.3V

7. Electrical Specifications

7.1 Power Supply DC Characteristics

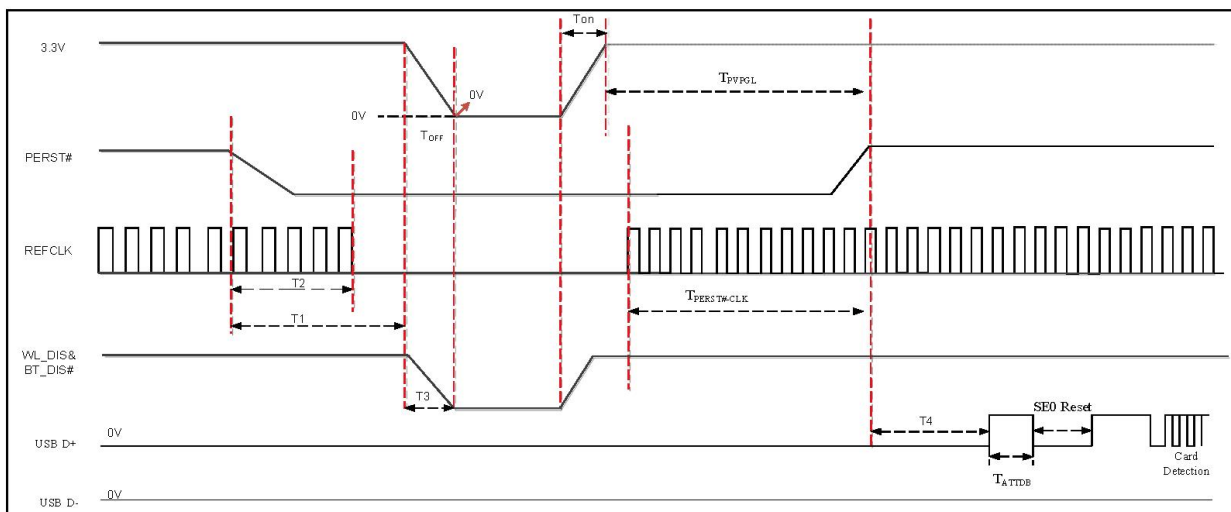
	MIN	TYP	MAX	Unit
Operating Temperature	0	25	70	deg.C
VDD33	3.0	3.3	3.6	V

7.2 Power Consumption

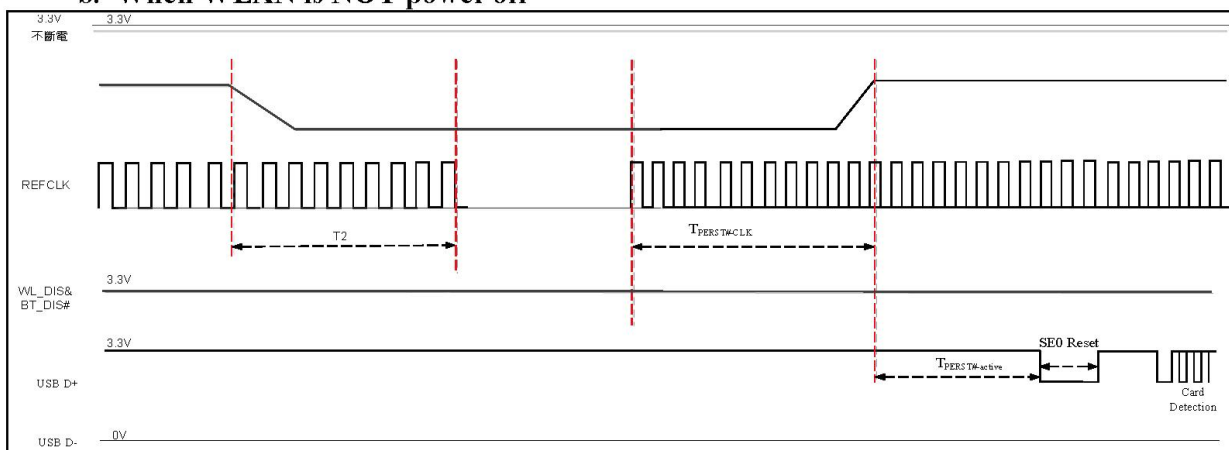
Power Consumption (Typical by using SWR)	Wi-Fi only: TBD
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7.3 PCIe Bus during Power On Sequence

a. When WLAN is power off



b. When WLAN is NOT power off



Ton: The main power ramp up duration

Toff: The main power off duration

TPVGL: Power valid to PERST# input inactive

TPERST#-CLK: Reference clock stable before PERST# inactive

TATTDB: the debounce interval with a minimal duration of 100ms that provided by the USB system Software

TSE0 Reset: USB host send SE0 Reset duration

TPERST#-active: PCI-e initial duration after PERST# inactive

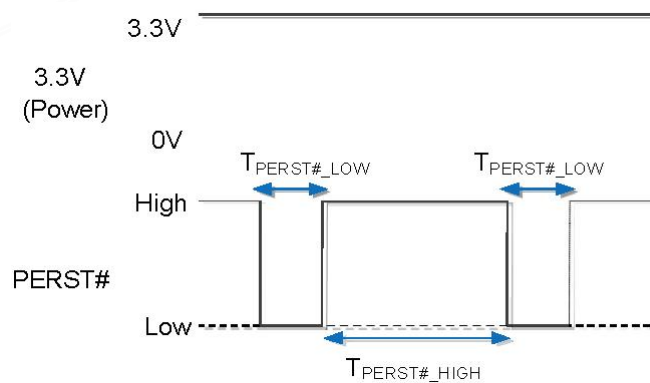
Note:

1. T1: PERST# goes active before the power on the connector is removed.
2. T2: Clock to inactive after PERST# goes active.
3. T3: WL_DIS# and BT_DIS# goes asserted when the power on the connector is removed.
4. T4: USB D+ go active after PERST# goes inactive.
5. T1/T2/T3/T4 timing value should large than 0.

Symbol	Unit	Min	Typical	Max
T_{on}	ms	0.5	1.5	5
T_{off}	ms	1.5		
T_{PVPGL}	ms	Implementation specific; recommended 50ms		--
T_{PERST#-CLK}	us	100	--	--
T_{ATTDB}	ms	100	--	--
T_{SE0 Reset}	ms	10	--	--
T_{PERST#-active}	ms	10	--	--

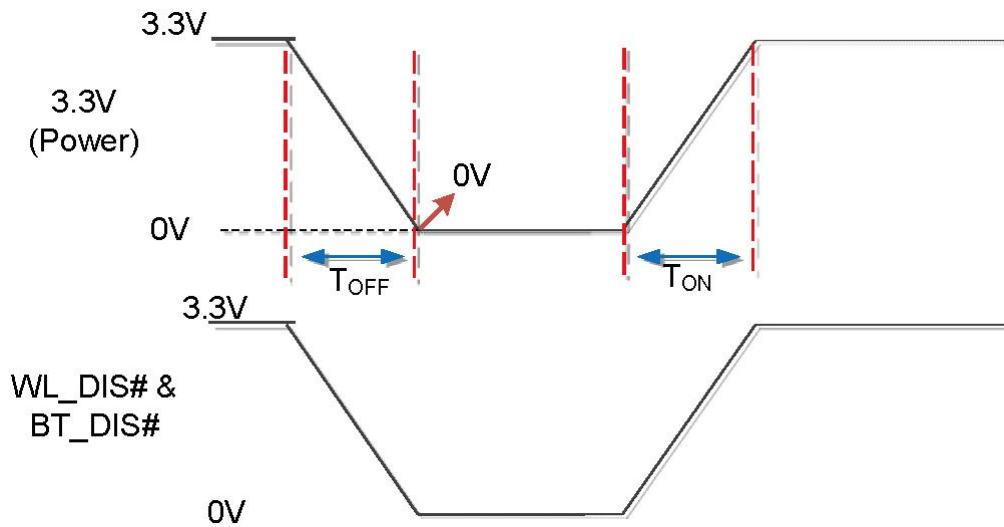
7.4 Interface Circuit time series

7.4.1 PCIe PERST# Timing Sequence (if need at least twice)



	Min	Typical	Max	Unit	Description
T _{PERST#_LOW}	6	10	X	ms	PERST# low duration
T _{PERST#_HIGH}	400	500	X	ms	PERST# high duration

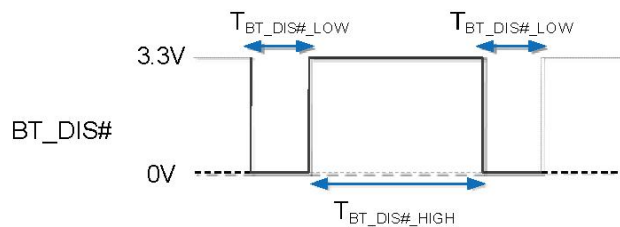
7.4.2 Power Off Sequence



Symbol	Min	Typical	Max	Unit	Description
T _{off}	1.5	-	-	ms	Measure point start on 100% Measure point end on 0% (must be 0V)
T _{on}	0.5	1.5	5	ms	Measure point start on 0% (must be 0V) Measure point end on 100%

Note: If BT_DIS# can't connect to the same power source with 3.3V, it need to be de-asserted before PERST# with 100ms in power on sequence.

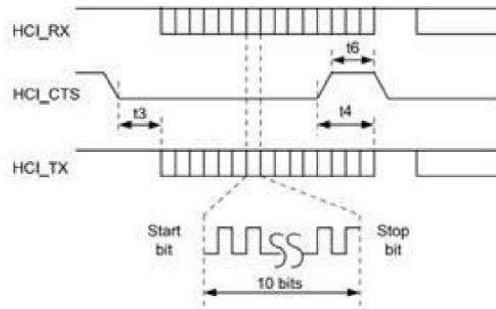
7.4.3 BT_DIS Timing Sequenece



	Min.	Typical	Max.	Unit	Description
BT_DIS#_LOW	200	--	--	ms	BT_DIS# low duration
BT_DIS#_HIGH	500	--	--	ms	BT_DIS# high duration

7.4.4 UART Interface Timing

The interface includes four signals, TXD/RXD/CTS. Flow control between the host and the device is byte-wise by hardware. When the UART_CTS signal is set high, the device stops transmitting on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.



UART Timing Diagram
UART Timing Characteristics

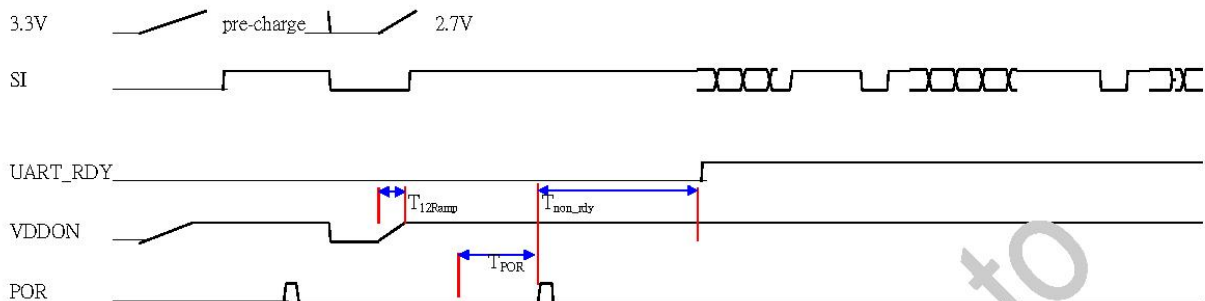
Parameter	Condition	Symbol	Min.	Typ	Max.	Unit
Baud rate			115.2		3000	Kbps
Baud rate accuracy per	Receive/Transmit		-3		3	%
CTS low to TX DATA on		T3	0	2		ns
CTS high to TX DATA off	Hardware flow	T4			1	byte
CTS High Pulse Width		T6	1			bit

Note : HCI packet means HCI command(256 bytes), HCI event(256 bytes), ACL(1024 bytes), SCO(256 bytes)

7.4.5 UART Interface Power-On Sequence

The UART interface power-on sequence differs depending on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported



UART Hardware Flow Control Supported

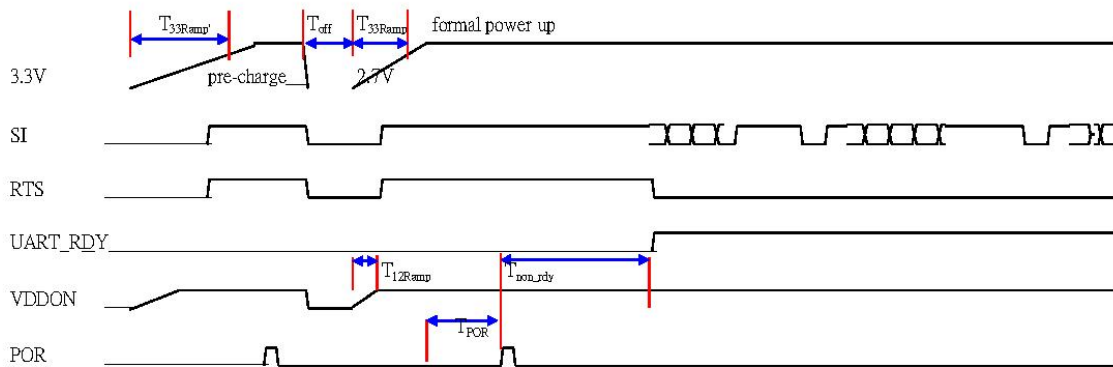


Figure 7. UART Power On Sequence With Hardware Flow Control

Table 20. UART Interface Power-On Sequence

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the RTL8852BE-VR-CG will not respond to any commands.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.


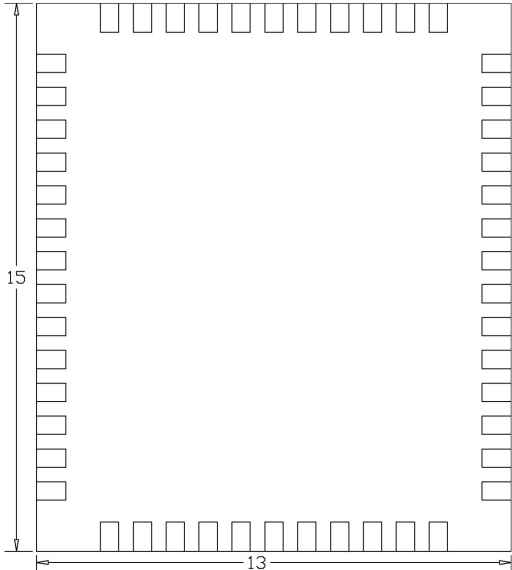
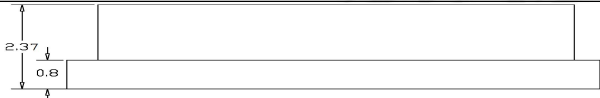
During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the Bluetooth block. The Bluetooth firmware then initializes all circuits included the UART.

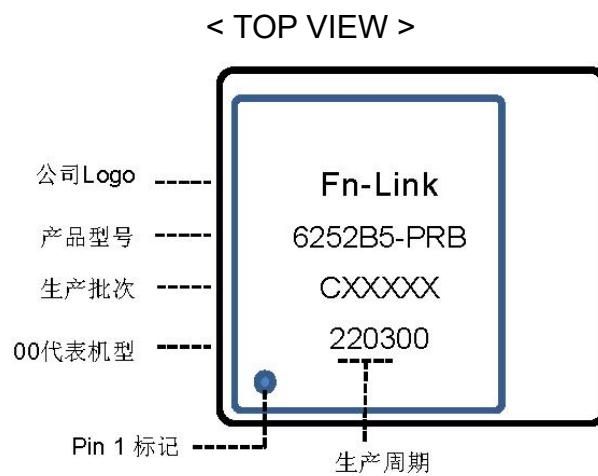
	Min.	Typical	Max.	Unit
T_{33ramp}	-	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
T_{non_rdy}	1	2	10	ms

8. Size reference

8.1 Module Picture

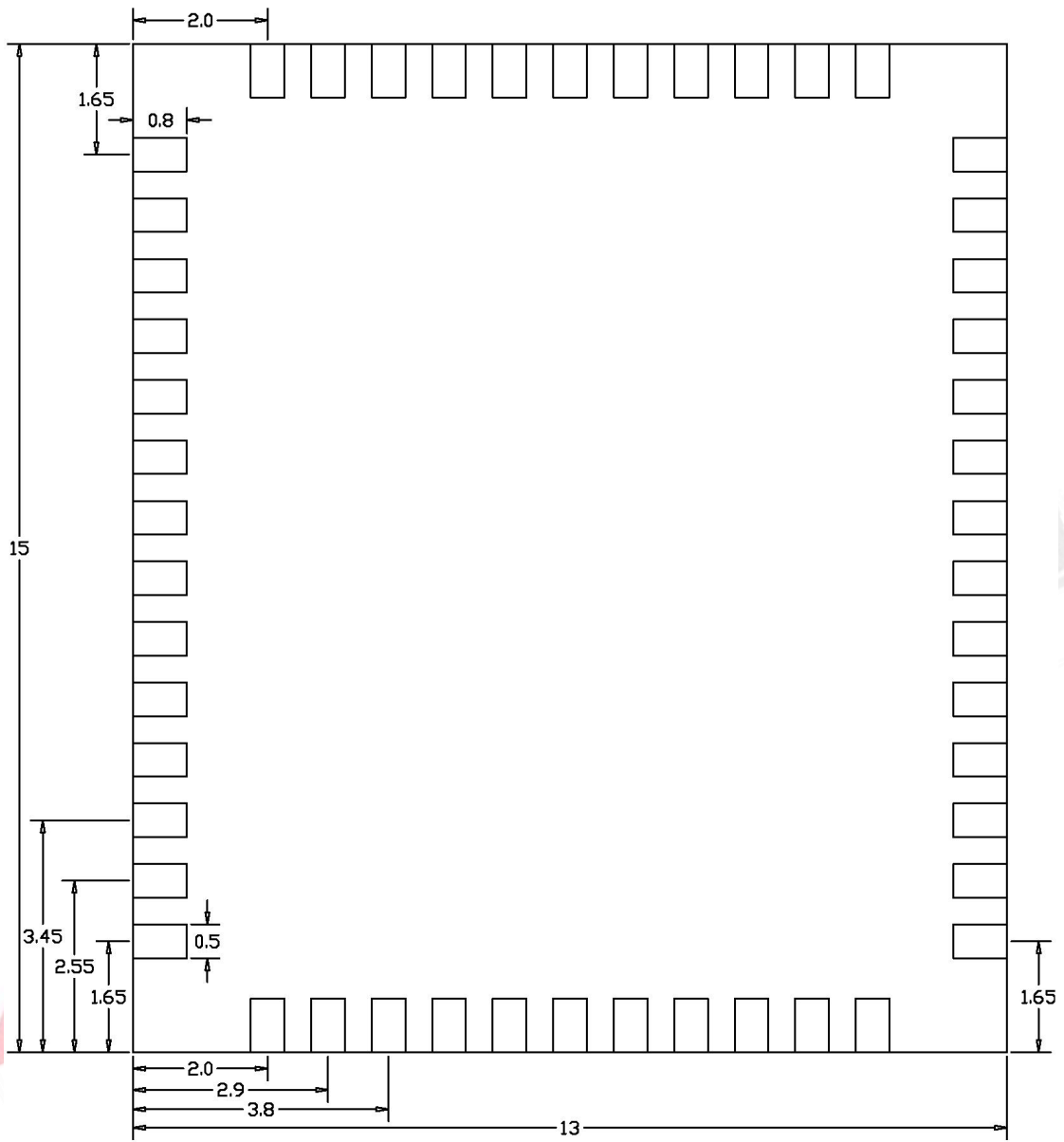
<p>L x W : 13 x 15 (+0.3/-0.1) mm</p> 	
<p>H: 2.37 (±0.2) mm</p>	
<p>Weight</p>	<p>0.97g</p>

8.2 Marking Description

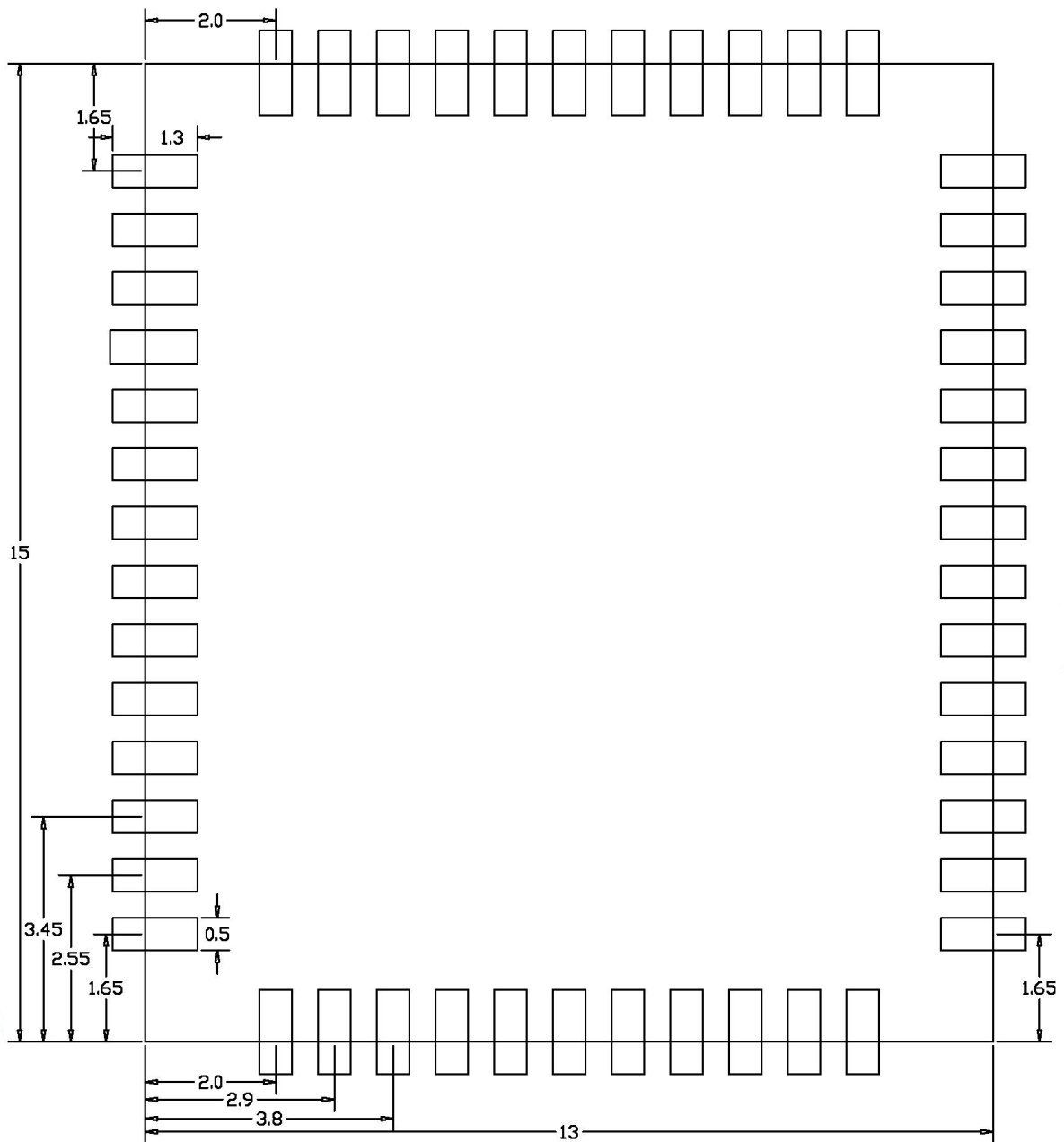


8.3 Physical Dimensions

<TOP View>



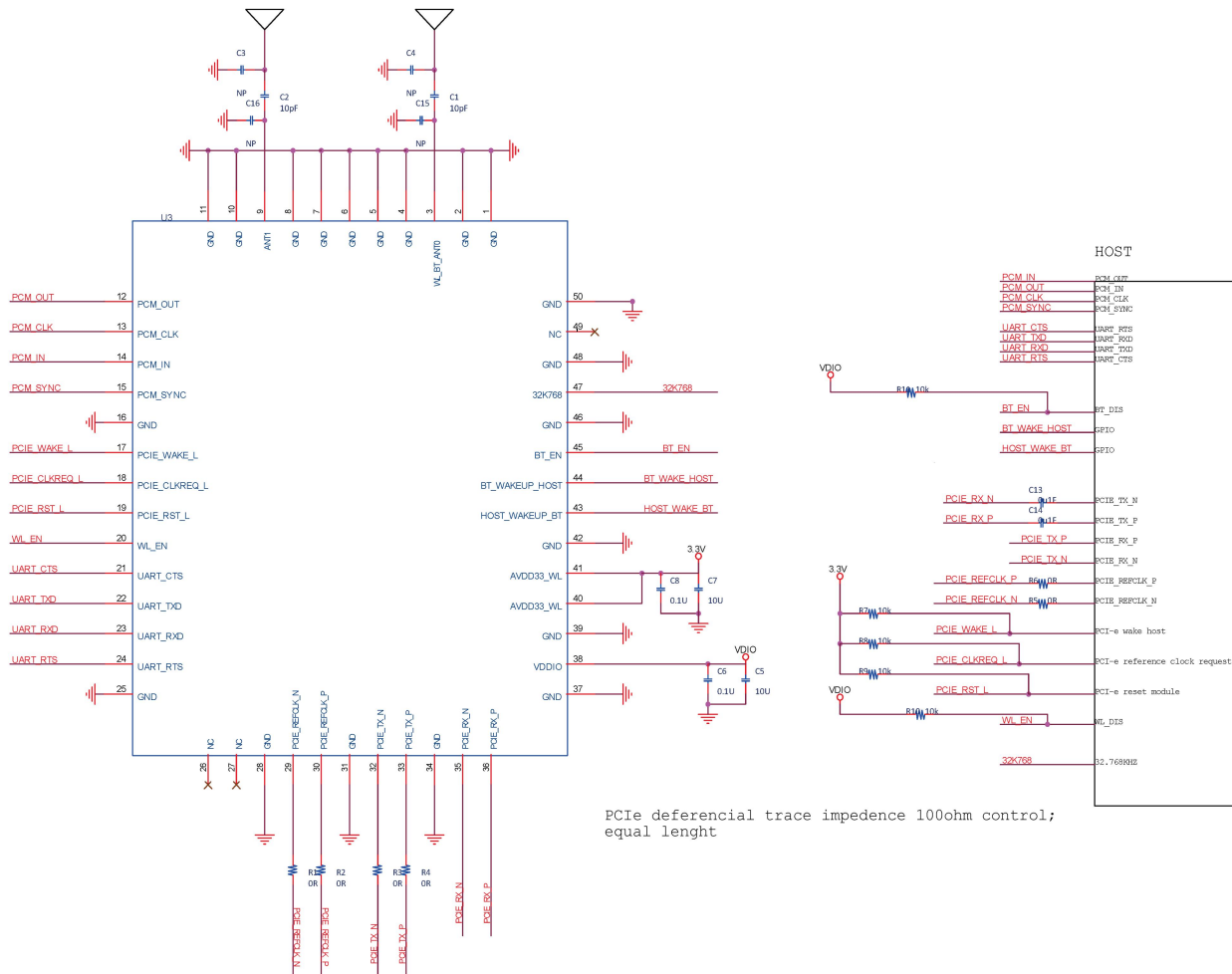
8.4 Layout Recommendation



9. The Key Material List

Item	Part Name	Description	Manufacturer
1	PCB	6252B5-PRB 绿色,4L,13X15X0.8mm	XY-PCB, GDKX, Sunlord, SLPCB
2	Crystal	2016 40MHz ±10ppm 12pF	ECEC, Hosonic, TKD, JWT
3	Chipset	RTL8852BE-VR-CG QFN76	Realtek
4	Shielding	6252B5-PRB Shielding	信太, 精力通

10. Reference Design

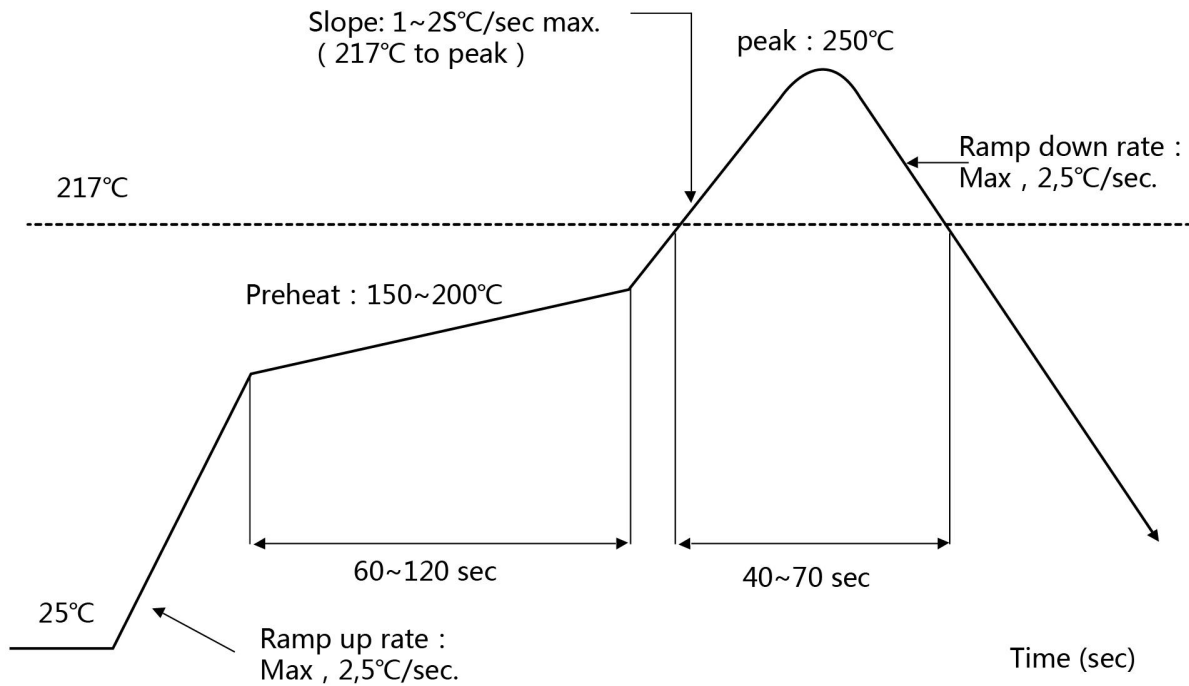


11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



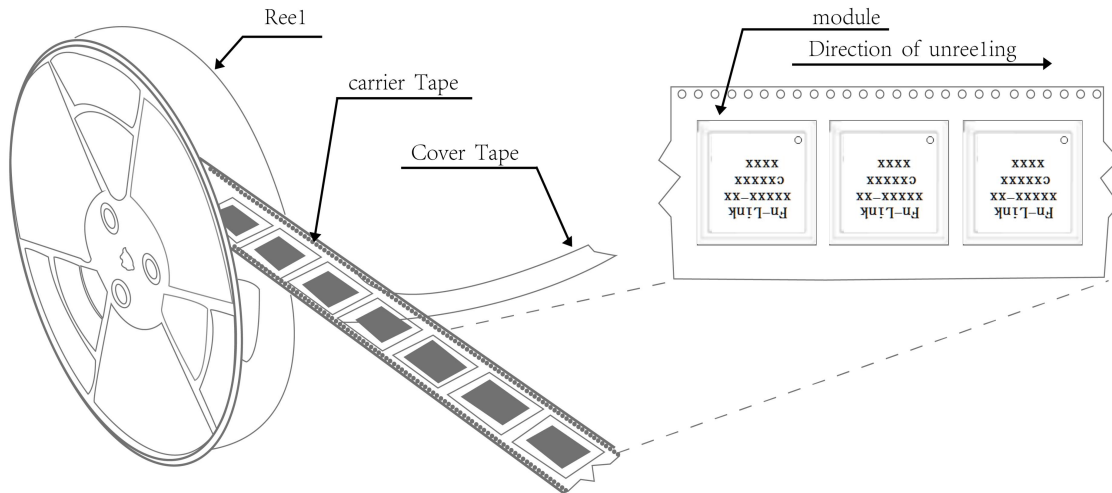
12. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

13. Package

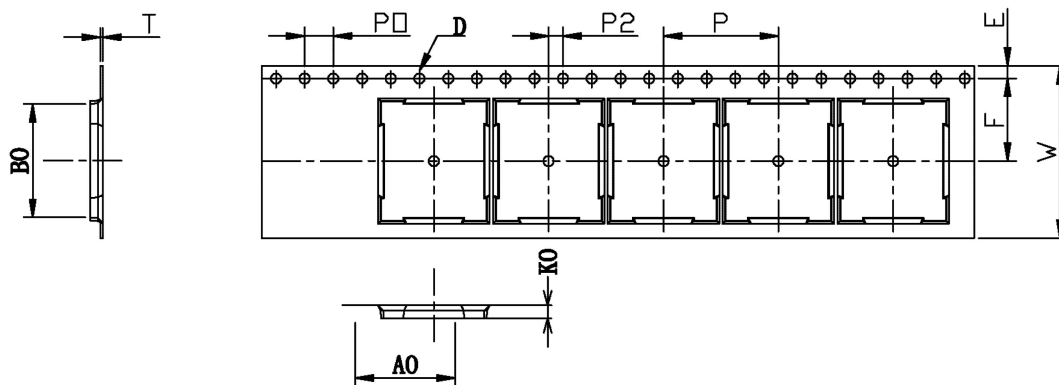
13.1 Reel

A roll of 1500pcs



13.2 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	13.40	15.40	1.50	11.5	1.75	2.65	4.0	2.0	16.0	0.30
TOLE	^{+0.3} _{-0.3}	±0.15	±0.15	^{+0.1} _{-0.0}	^{+0.1} _{-0.1}	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



13.3 Packaging Detail

the take-up package



Using self-adhesive tape

Size of black tape: 24mm*24.4m the cover tape :21.3mm*32.6m

Color of plastic disc: blue



NY bag size:450mm*415mm



size : 350*350*35mm



The packing case size:360*210*370mmg

14. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <math><40^{\circ}\text{C}</math> and <math><90\%</math> relative humidity (RH)
- b) Environmental condition during the production: - c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- d) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected
- e) Baking is required if conditions b) or c) are not respected
- f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more