FN-LINK欧智通

PRODUCT SPECIFICATION

F89FTSM13

Wi-Fi Single-band 1T1R Module Datasheet

Version:v1.2

F89FTSM13 Module Datasheet

	Part NO.	Description
Ordering Information	FG89FTSM13-W9	RTL8189FTV-VQ1,802.11b/g/n,1T1R,12.0*12.0 ,SDIO2.0/Uart,with shielding.PCB v04

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL:+86-755-2955-8186 Website:www.fn-link.com

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Revision History

Version	Date	Contents of Revision Change	Draft	Checked	Approved
V1.0	2020/7/16	First Released	LXY	LXY	SZS
V1.1	2021/2/19	Update size tolerance to +/-0.4mm	LXY	LXY	SZS
V1.2	2022/1/15	Update the specification format Update Reference Design	FC	LXY	QJP

1. General Description

1.1 Introduction

F89FTSM13 is a highly integrated and excellent performance Wireless LAN (WLAN) SDIO network interface device. High-speed wireless connection up to 72.2 Mbps.

The general hardware for the module is shown in Figure 1. This WLAN Module design is based on Realtek RTL8189FTV. It is a highly integrated single-chip 1*1 SISO Wireless LAN (WLAN) SDIO network interface controller complying with the 802.11n specification. It combines a MAC, a 1T1R capable baseband, and RF in a single chip. It is designed to provide excellent performance with low power Consumption and enhance the advantages of robust system and cost-effective.

1.2 Description

Model Name	F89FTSM13
Product Description	Support Wi-Fi functionalities
Dimension	L x W x H: 12 x 12 x1.8 mm
Wi-Fi Interface	Support SDIO/GPIO
OS supported	Android /Linux
Operating temperature	0°C to 70°C
Storage temperature	-40°C to 80°C

2. Features

General

- Enterprise level security which can apply WPA/WPA2 certification for WiFi

PHY Features

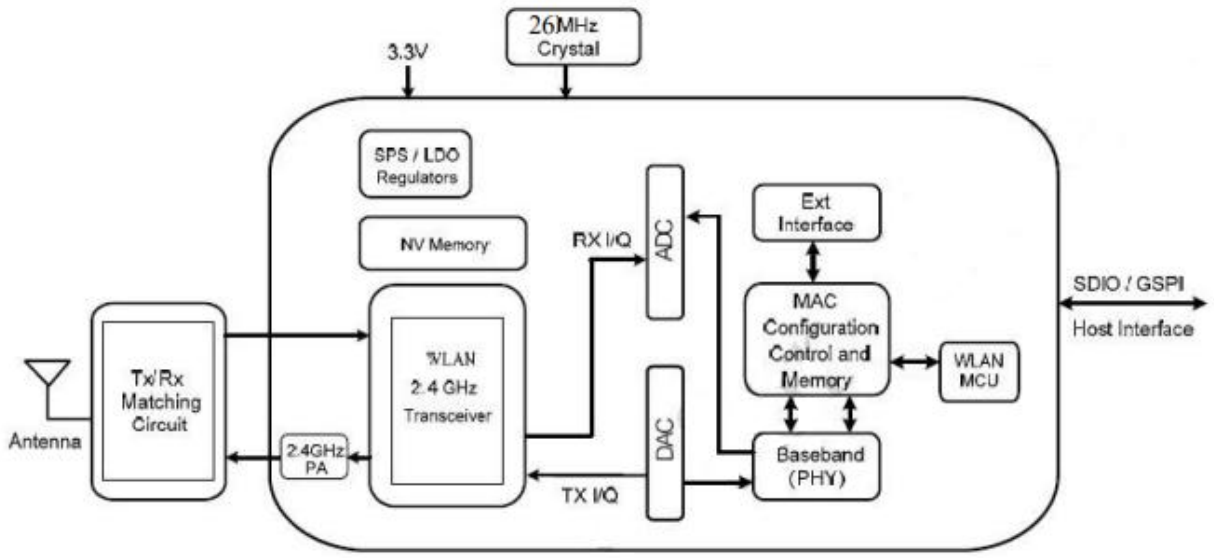
- Operate at ISM frequency bands (2.4GHz)
- IEEE standards support: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n
- WiFi 1 T 1 R allow data rates supporting up to 72.2Mbps downstream and upstream PHY rates

Host Interface

- SDIO V1.1/2.0 Interface for WiFi

3. Block Diagram

Single-Band 11n (1x1) Solution



4. General Specification

4.1 WI-FI Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.4 GHz ~ 2.497 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 16dBm ± 2 dB	EVM ≤ -10dB
	802.11g /54Mbps : 14dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 13dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 11Mbps PER @ -84 dBm	≤-76
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 54Mbps PER @ -72 dBm	≤-68
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=7 PER @ -67 dBm	≤-65

5. ID setting information

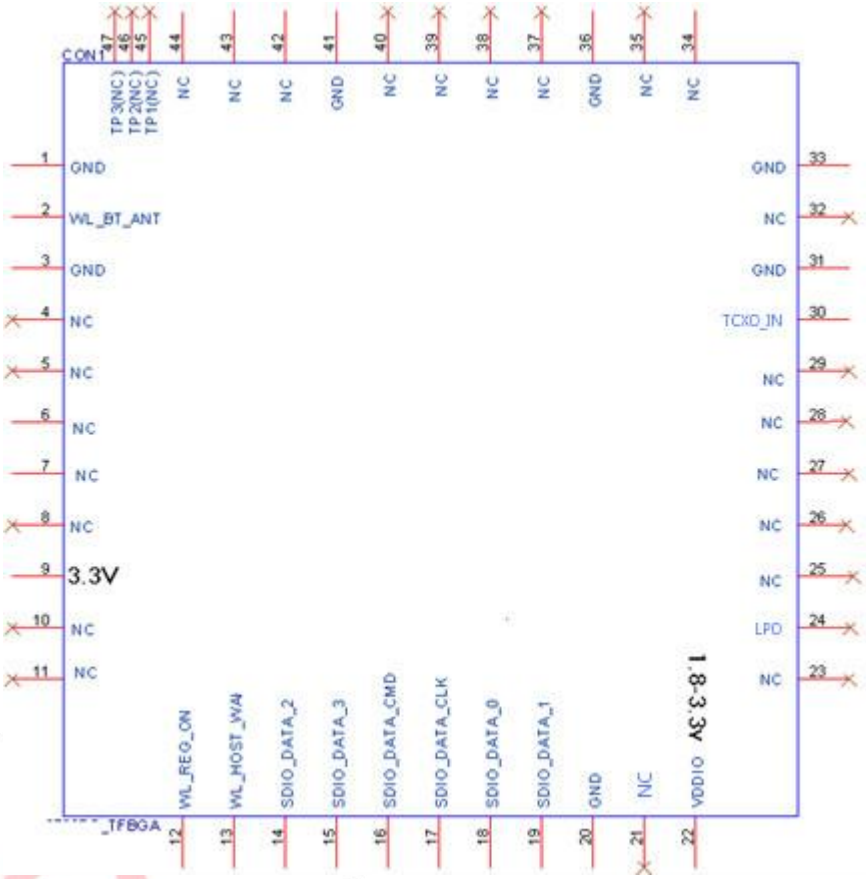
WI-FI

Vendor ID	-
Product ID	-

6. Pin Definition

6.1 Pin Outline

< TOP VIEW >



6.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND		Ground connections	
2	RF	I/O	RF OUTPUT	
3	GND		Ground connections	
4~8	NC		Floating (NC)	
9	3.3V	P	3.3V	3.3V
10	NC		Floating (NC)	

11	NC		Floating (NC)	
12	WL_REG_ON		Chip_EN, external pull low shutdown RTL8189FTV	3.3V
13	WL_HOST_WAKE	O	WLAN WAKE HOST	
14	SDIO_DATA_2	I/O	SDIO_D2	
15	SDIO_DATA_3	I/O	SDIO_D3	
16	SDIO_DATA_CMD	I/O	SDIO_CMD	
17	SDIO_DATA_CLK	I	SDIO_CLK	
18	SDIO_DATA_D0	I/O	SDIO_D0	
19	SDIO_DATA_D1	I/O	SDIO_D1	
20	GND		Ground connections	
21	NC		Floating (NC)	
22	VDIO		1.8 or 3.3V	
23	NC		Floating (NC)	
24	LPO		CLK_REQ, not used please NC.	
25	NC		Floating (NC)	
26~29	NC	P	Floating (NC)	
30	TCXO_IN		26MHz_IN, not used please NC.	
31	GND		Ground connections	
32	NC		Floating (NC)	
33	GND		Ground connections	
34~35	NC		Floating (NC)	
36	GND		Ground connections	
37~40	NC		Floating (NC)	
41	GND		Ground connections	
42~44	NC		Floating (NC)	

7. Electrical Specifications

7.1 Power Supply DC Characteristics

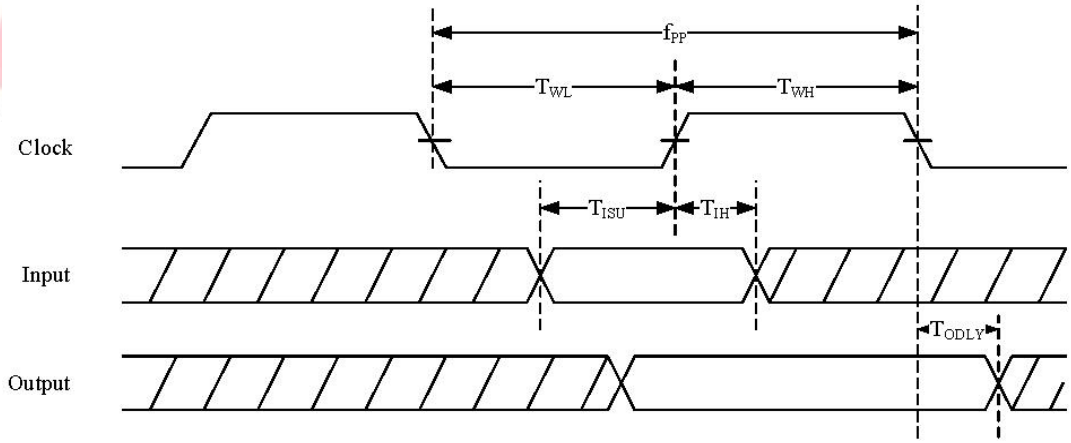
	MIN	TYP	MAX	Unit
Operating Temperature	0	25	70	deg.C
VCC33	3.0	3.3	3.6	V
VDDIO	1.62	1.8 or 3.3	3.6	V

7.2 Power Consumption

Mode	Status	Power(mA)	Note
OS Windows XP	Link	130	
	RX	130	20M
	TX	190	20M(MCS7)

7.3 Interface Circuit time series

7.3.1 SDIO/GSPI Interface Timing



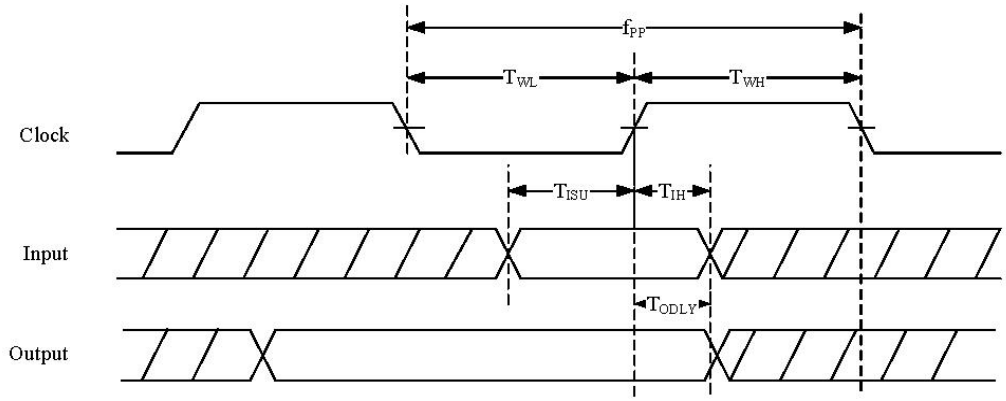


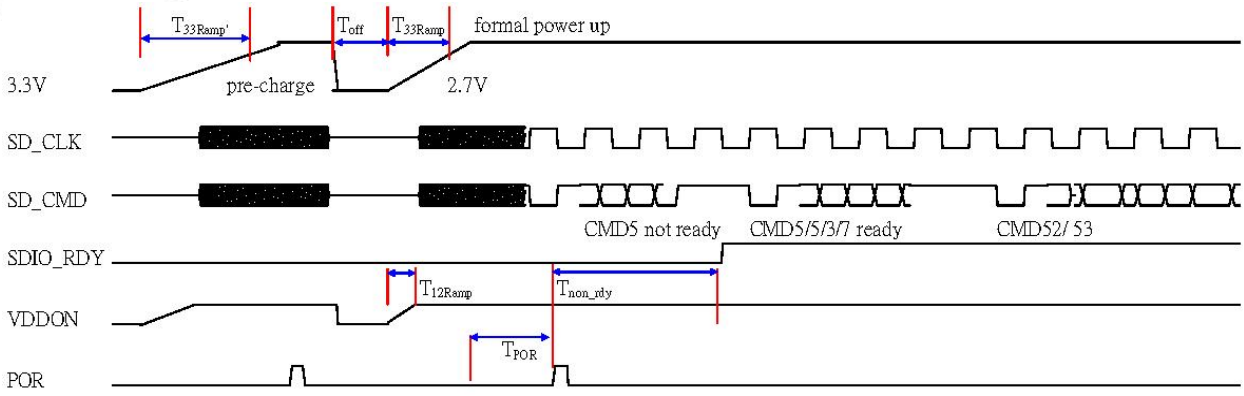
Figure 4. SDIO High Speed Interface Timing

Table 11. SDIO/GSPI Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns

7.3.2 SDIO Interface Power-On Sequence

After power-on, the SDIO interface is selected by the RTL8189FTV-VC automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power-on sequence is recommended:



Variable definition:

$T_{33ramp'}$: The 3.3V power pre-charge ramp up duration before formal power up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power-on sequence. This procedure can eliminate the host card detection issue when the power ramp up duration is too long or the system warm reboot fails.

T_{off}: The duration 3.3V is cut off before formal power up.

T_{33ramp}: The 3.3V main power ramp up duration.

T_{12ramp}: The internal 1.2V ramp up duration.

T_{POR}: The duration the power-on reset releases, and the power management unit executes power-on tasks. The power-on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.

T_{non_rdy}: SDIO not ready duration. In this state the RTL8189FTV-VC may respond to commands without the ready bit set. After the ready bit is set, the host will initiate the full card detection procedure.

Power-On Flow Description

We recommend that the card detection procedures are divided into two phases: a 3.3V power pre-charge phase and a formal power-up phase.

For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after a Toff period. The ramp up time is specified by the T33ramp duration.

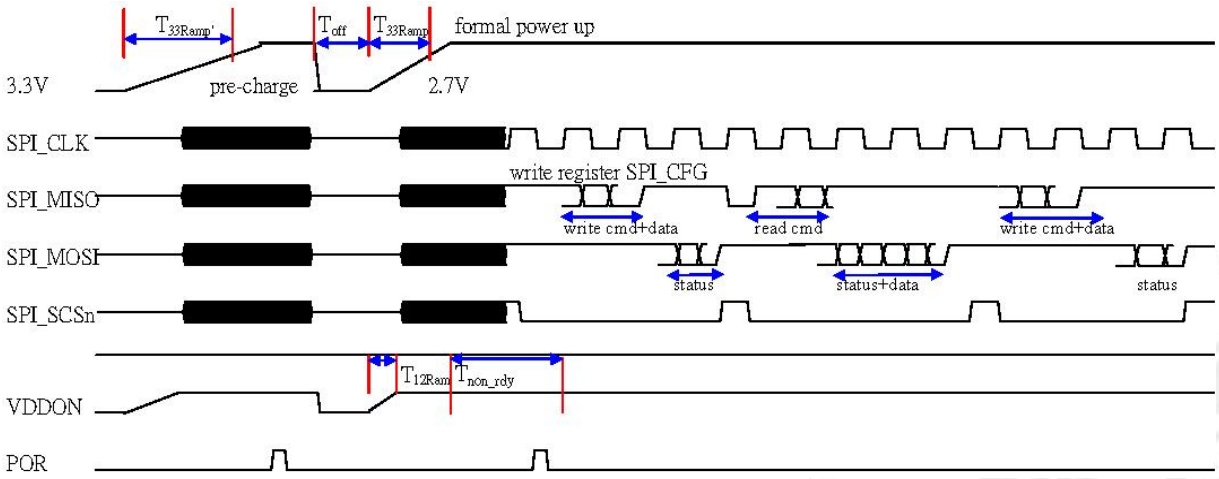
After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by the power ready detection circuit, and will enable the SDIO block. eFUSE is then autoloaded to the SDIO circuits during the Tnon_rdy duration. After the autoload has completed, the SDIO sets the ready bit. After CMD5/ 5/3/7 procedures, card detection is then executed. After the driver has loaded, normal commands 52 and 53 are then used.

A typical timing specification is shown below:

Parameter	Min	Typical	Max	Unit
$T_{33ramp'}$	0.25	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.25	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
$T_{non-rdy}$	1	2	10	ms

7.3.3 GSPI Interface Power-On Sequence

The GSPI interface is enabled automatically when a valid GSPI command is first received. The recommended power-on sequence is as follows:



Definitions

$T_{33ramp'}$: The 3.3V power pre-charge ramp up duration before formal power up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power-on sequence. This procedure can eliminate the host card detection issue when the power ramp up duration is too long or the system warm reboot fails.

T_{off}: The duration 3.3V is cut off before formal power up.

T_{33ramp}: The 3.3V main power ramp up duration.

T_{12ramp}: The internal 1.2V ramp up duration.

T_{non_rdy}: The duration of SPI device internal initialization. After Tnon_rdy, the SPI host can then send commands to write the SPI_CFG register. The SPI_CFG register controls SPI endian and word length.

Power-On Flow Description

We recommend that the card detection procedures are divided into two phases: a 3.3V power pre-charge phase and a formal power-up phase.

For the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V is then cut off and is turned on after a Toff period. The ramp up time is specified by the T33ramp duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit will be enabled by the power ready detection circuit, and will enable the SPI block. eFUSE is then autoloaded to the SPI circuits, and the internal power circuits are configured during the Tnon_rdy duration.

A typical timing specification is shown below:

Parameter	Min	Typical	Max	Unit
$T_{33ramp'}$	0.25	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.25	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
$T_{non\text{-}rdy}$	3	4	18	ms

7.3.4 SDIO Interface

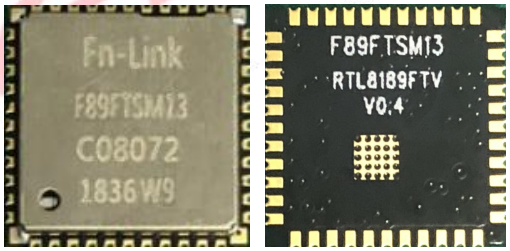
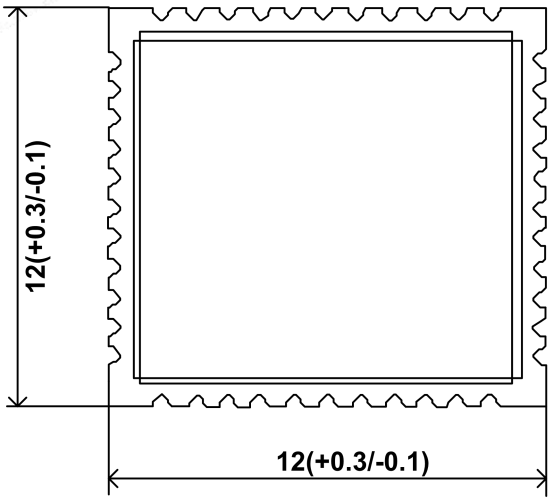
Symbol	Type	Pin	Description
SD_CLK	I	16	SDIO Clock Input
SD_CMD	I/O	15	SDIO Command Input
SD_D0	I/O	17	SDIO Data Line 0
SD_D1	I/O	18	SDIO Data Line 1
SD_D2	I/O	13	SDIO Data Line 2
SD_D3	I/O	14	SDIO Data Line 3

7.3.5 GPIO Interface

Symbol	Type	Pin	Description
GSPI_CLK	I	16	GSPI Clock Input
GSPI_MOSI	I	15	GSPI Data Input
GSPI_MISO	O	17	GSPI Data Out
GSPI_SIRQ	O	18	GSPI Interrupt
GSPI_SCSn	I	14	GSPI Chip Select Bar

8. Size reference

8.1 Module Picture

<table>
<tr><td>L x W : 12 x 12 (+0.3/-0.1) mm
 
</td><td> 
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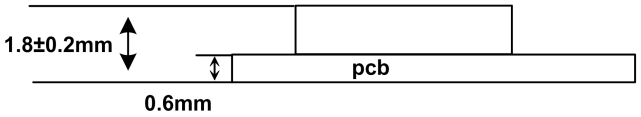
<tr><td>H: 1.8 (±0.2) mm</td><td> 
</td></tr>
<tr><td>Weight</td><td>TBD</td></tr>
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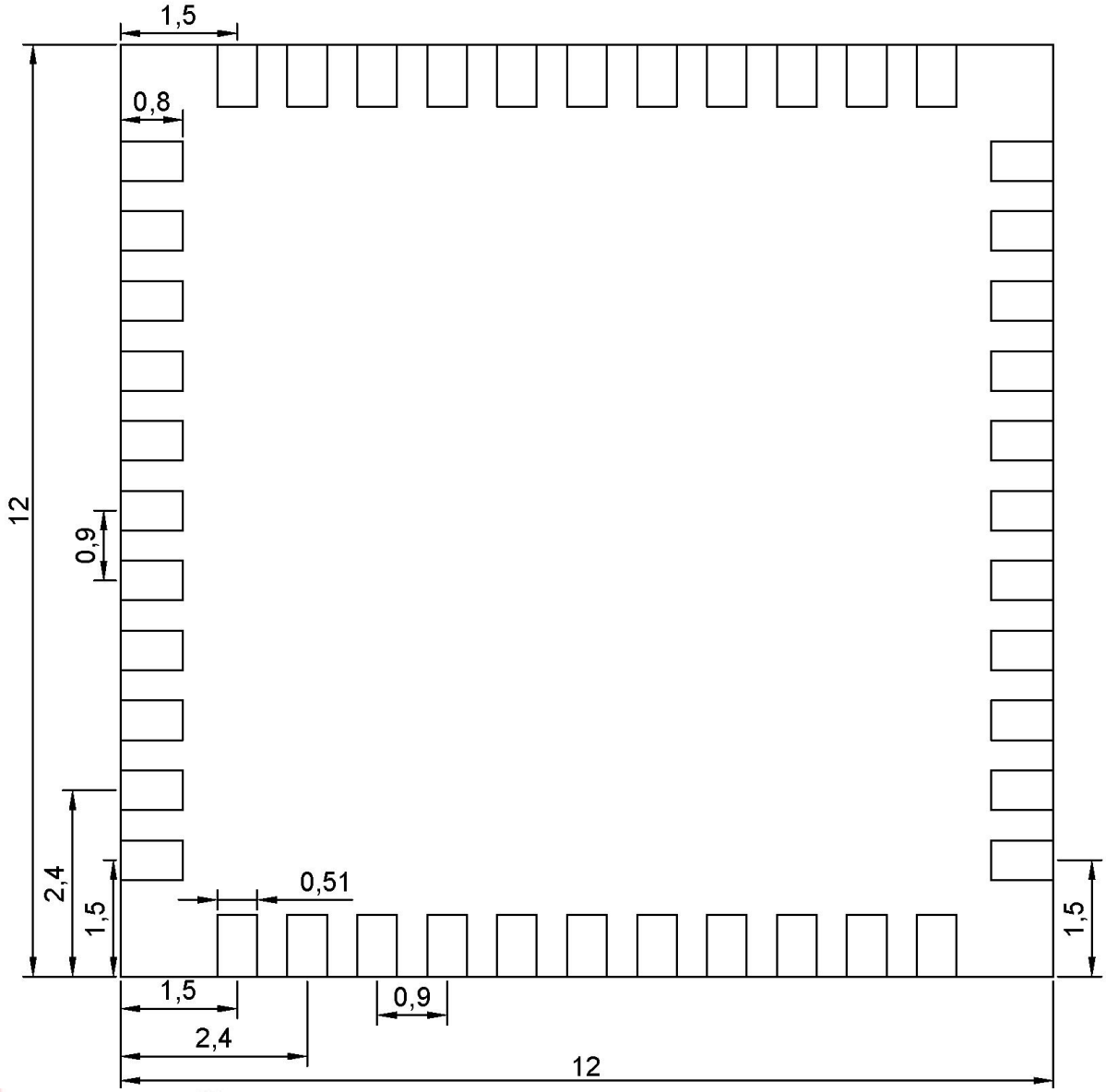
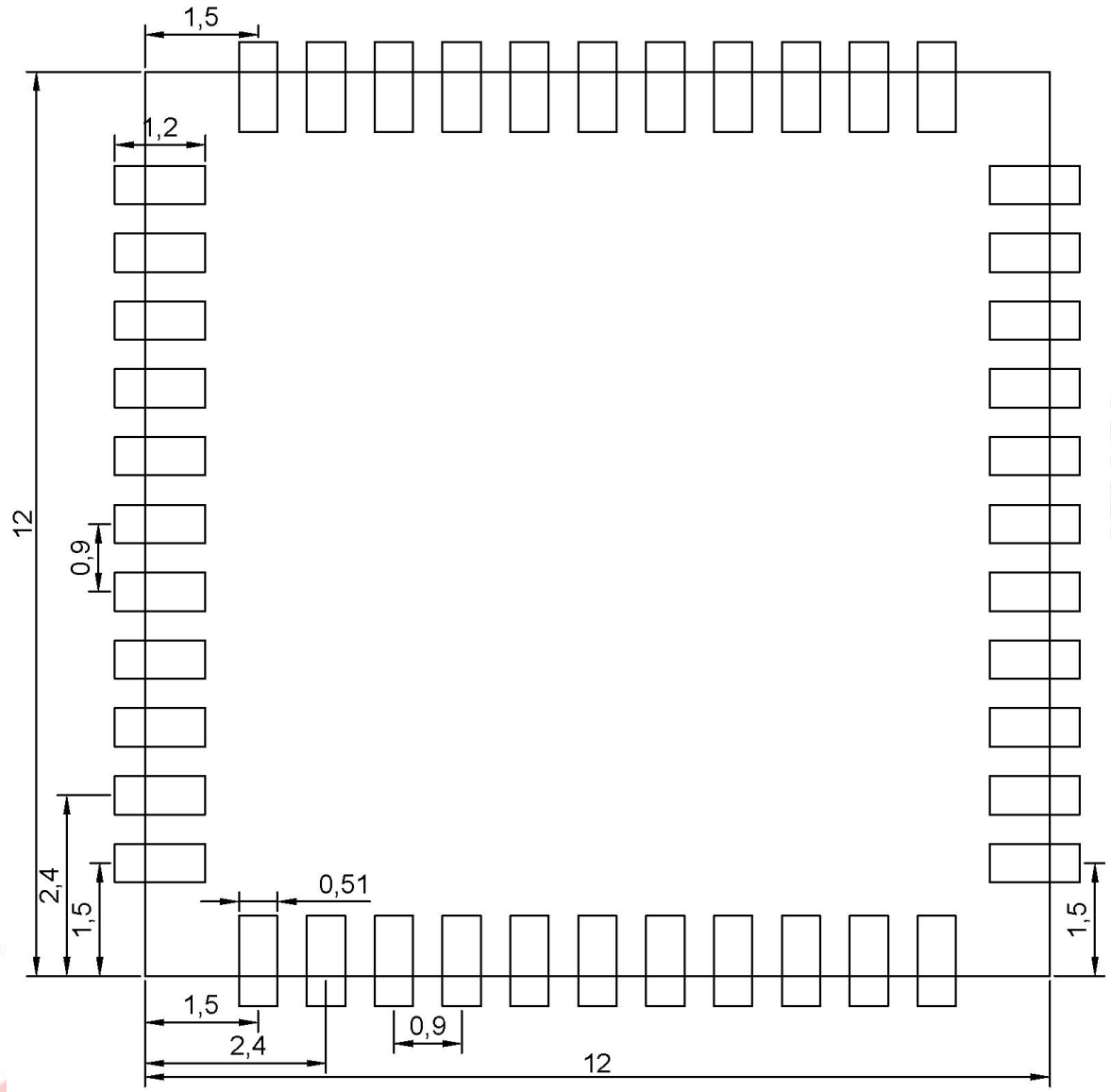
8.2 Physical Dimensions

<TOP View>



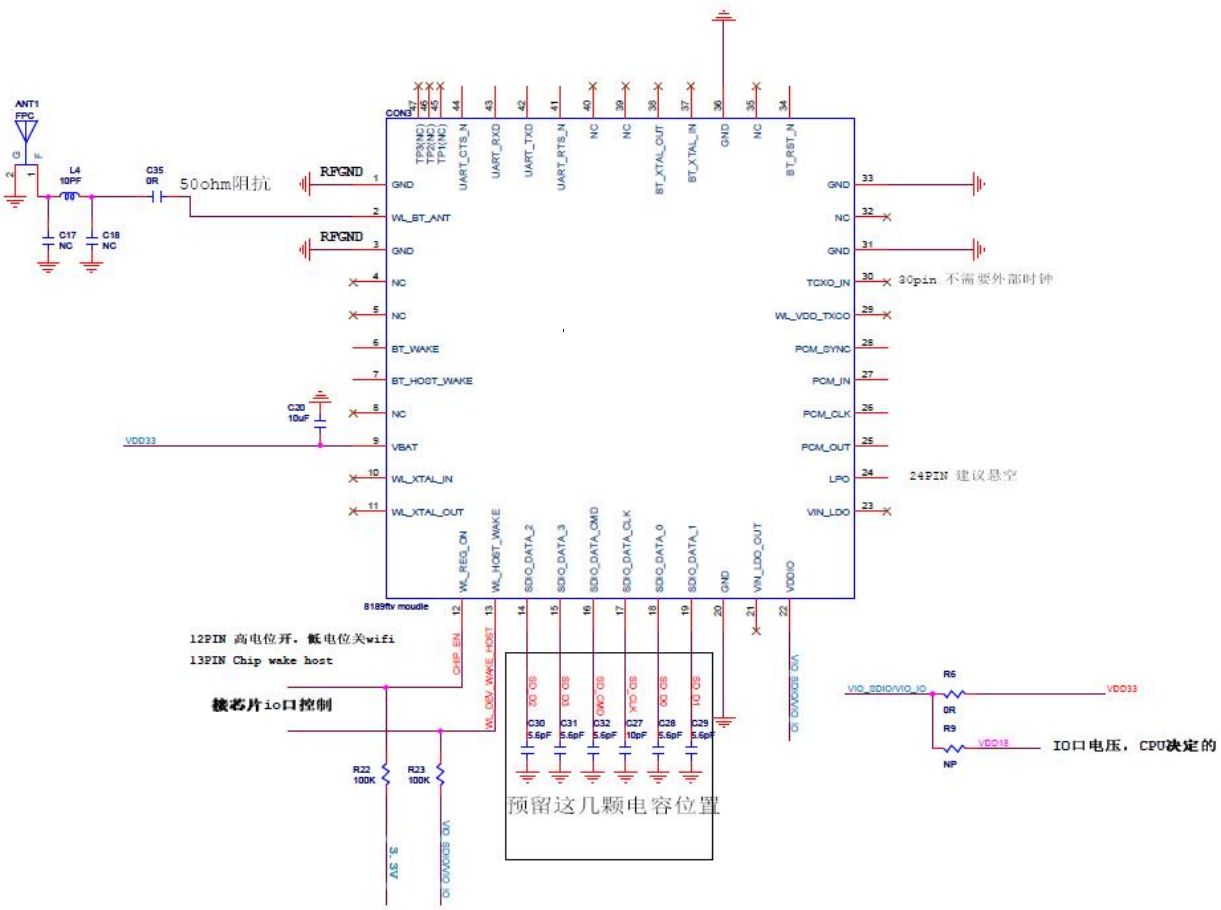
8.3 Layout Recommendation



9. The Key Material List

Item	Part Name	Description	Manufacturer
1	IC	RTL8189FTV -VQ1-CG	REALTEK
2	Crystal	26mhz ±10ppm,10.5pF,3225	ECEC,HOSONIC,TKD,JWT
3	PCB	F89FTSM13 12X12 4L	XY-PCB,KX-PCB,SL-PCB,Sunlord
4	TVS	ESD 0402 5.5V 0.1pF	Sunlord,Murata,way-on
5	Shielding	F1023XM13-W1shielding	信太，精力通

10. Reference Design

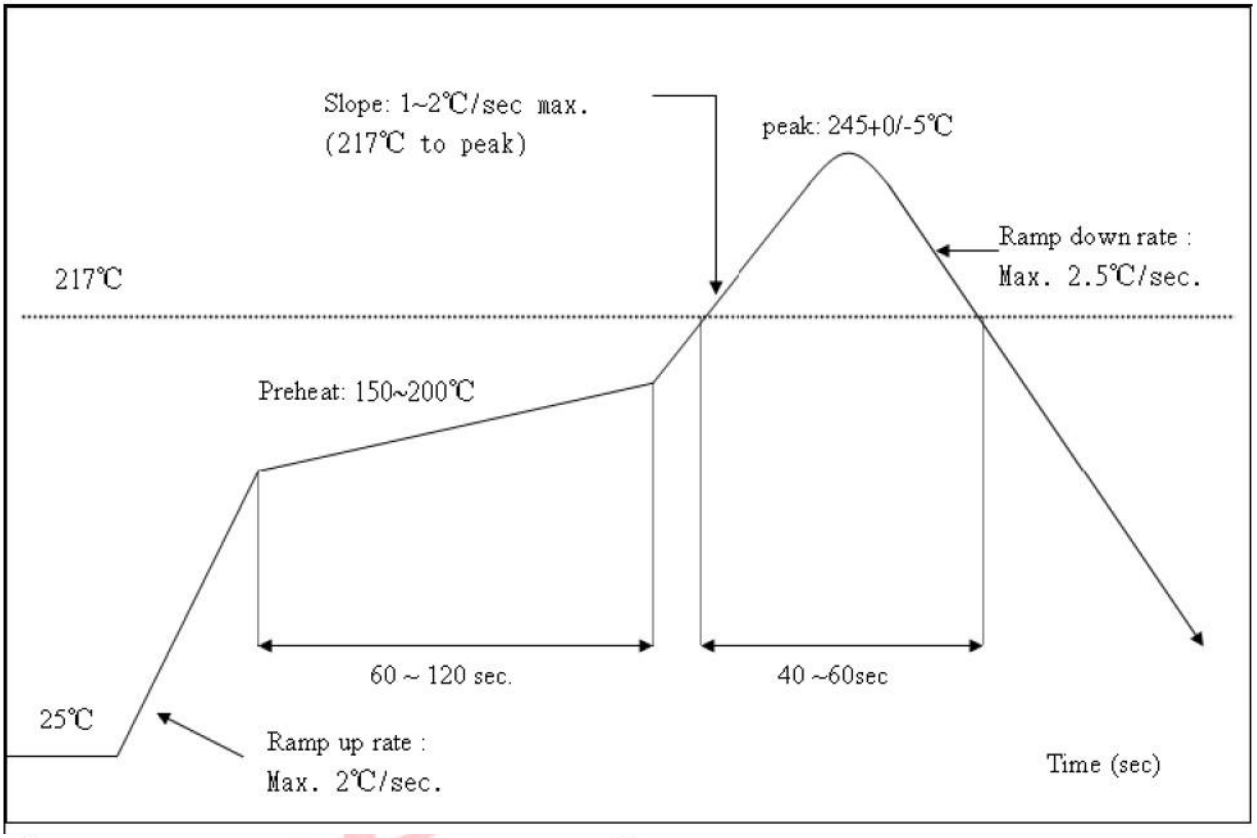


11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times

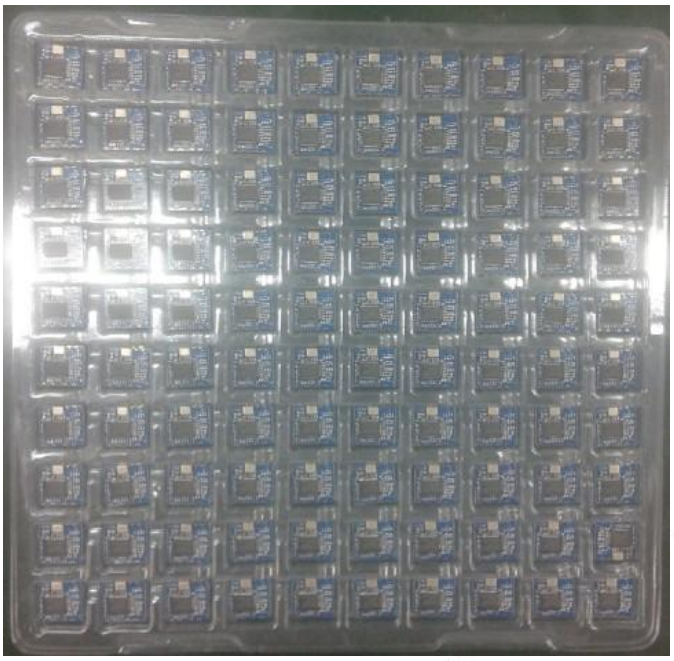


WIFI module installed note:

1. Please press 1 : 1 and then expand outward proportion to 0.7 mm, 0.12 mm thickness When open a stencil
2. Take and use the WIFI module, please insure the electrostatic protective measures.
3. Reflow soldering temperature should be according to the customer the main size of the products, such as the temperature set at 250 + 5 ℃ for the MID motherboard

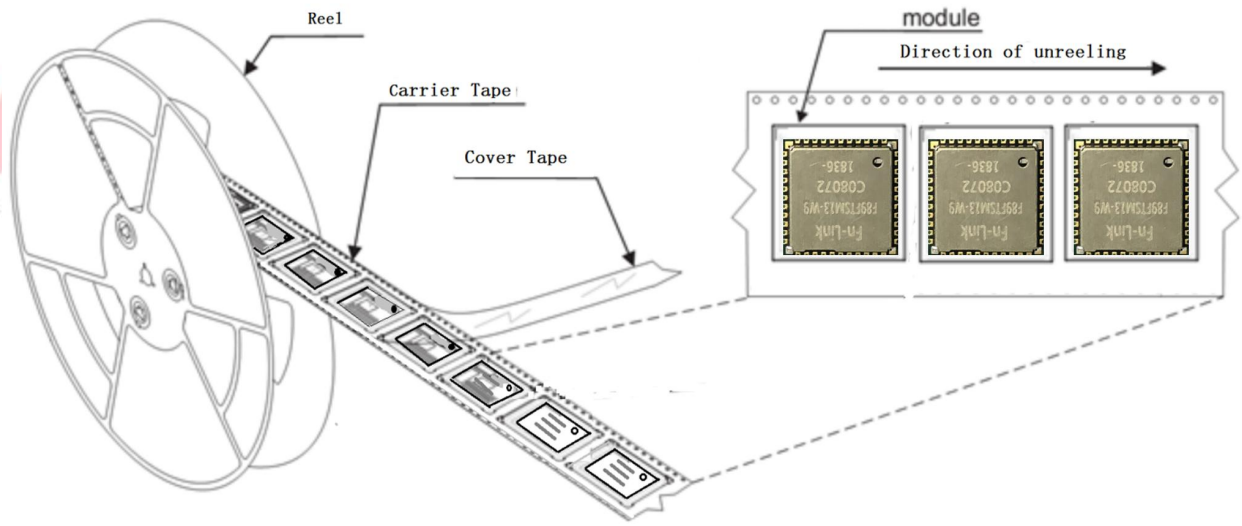
12. Package

12.1 Blister packaging



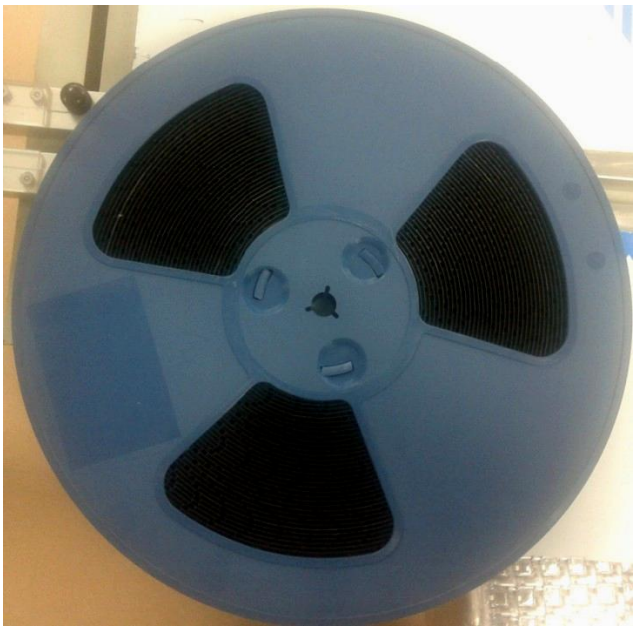
12.2 Reel

A roll of 1500pcs



12.3 Packaging Detail

the take-up package



13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more