FN-LINK 欧智通

PRODUCT SPECIFICATION

L297B-SR

Wi-Fi Dual-band 2x2 11ac+ Bluetooth 5.0

Combo Module

Version:v1.2

L297B-SR Module Datasheet

Ordering Information	Part NO.	Description
	FGL297BSRX-00	NXP88W8997, b/g/n/ac, Wi-Fi+BLE5.0, 2T2R, 13X15mm, SDIO/ UART, PCB version V1.0

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

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Revision History

Version	Date	Contents of Revision Change	Preparde	Checked	Approved
V1.0	2021/11/19	New version	FC	Tzq	Qjp
V1.1	2022/01/19	Add Module picture Revision pin definition Add marking description	FC	Tzq	Qjp
V1.2	2022/02/15	Update ping outline	FC		

1. General Description

1.1 Introduction

This document is to specify the product requirements for 802.11a/b/g/n/ac and Bluetooth 5.0 SDIO&UART module. This module based on NXP(MARVELL) 88W8997 chipset that complied with IEEE 802.11a, IEEE 802.11b, IEEE 802.11g, IEEE 802.11n, IEEE 802.11ac standard from 2.4~2.5GHz and 5.15GHz ~ 5.85GHz, and it also can be used to provide up to 11Mbps for IEEE 802.11b, 54Mbps for IEEE 802.11a and IEEE 802.11g, 150Mbps for 802.11n and 866.7Mbps for IEEE 802.11ac to connect your wireless LAN.

1.2 Description

Model Name	L297B-SR
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 13 x 15 x2.3 mm
Wi-Fi Interface	Support SDIO V2.0/3.0
BT Interface	UART/SDIO
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	-30°C to 85°C
Storage temperature	-55°C to 125°C

2. Features

General

- Compatible with IEEE 802.11a standard to provide wireless 54Mbps data rate
- Compatible with IEEE 802.11b standard to provide wireless 11Mbps data rate
- Compatible with IEEE 802.11g standard to provide wireless 54Mbps data rate
- Compatible with IEEE 802.11n standard to provide wireless 150Mbps data rate
- Compatible with IEEE 802.11ac standard to provide wireless 866.7Mbps data rate
- Supports TKIP/WEP, AES/CCMP, AES/CMAC, AES/GCMP and WAPI enhanced security

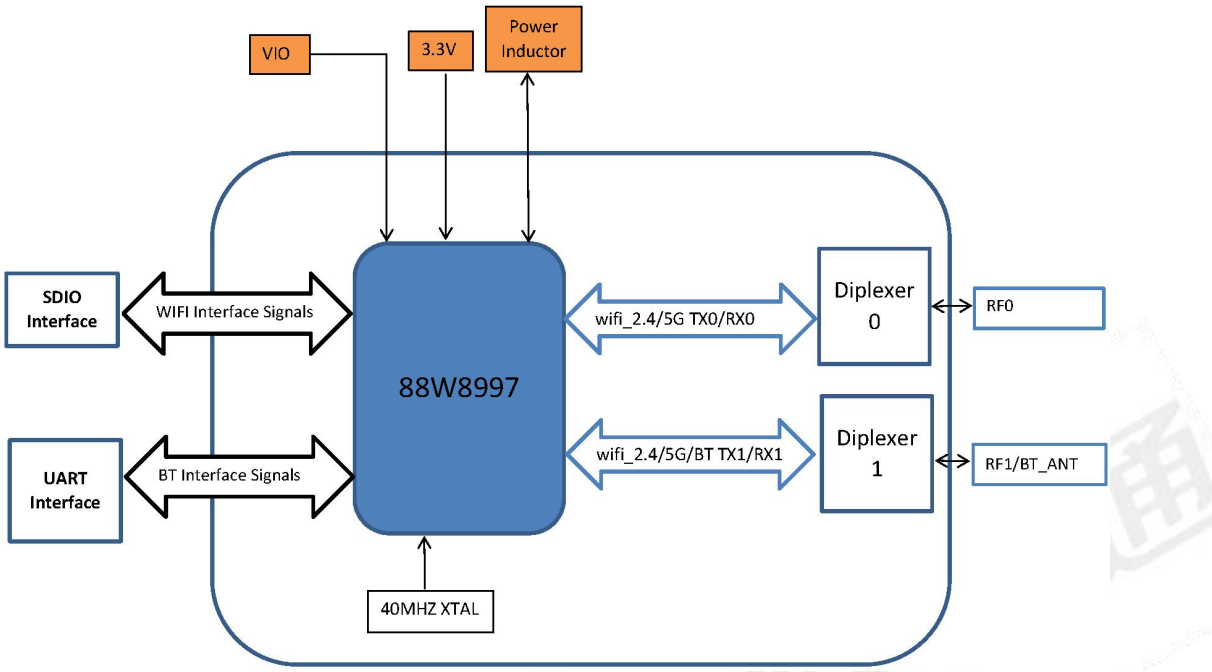
Host Interface

- SDIO 2.0/3.0 Interface for WLAN
- SDIO Interface or High-Speed UART Interface for Bluetooth
- HSF compliant

Bluetooth Features

- Bluetooth 5.0 compliant
- Supports Bluetooth classic (BDR/EDR)
- Supports Bluetooth Low Energy (BLE)

3. Block Diagram



4. General Specification

4.1 2.4GHz WI-FI Specification

Feature	**Description**	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 16dBm ± 2 dB	EVM ≤ -10dB
	802.11g /54Mbps : 15dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
Receive Sensitivity (11b,20MHz) @8% PER	- 11Mbps PER @ -83 dBm	≤-76

Receive Sensitivity (11g,20MHz) @10% PER	- 54Mbps PER @ -74 dBm	≤-65
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=7 PER @ -68 dBm	≤-64
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=7, PER @ -66 dBm	≤-61

4.2 5GHz WI-FI Specification

Feature	**Description**	
WLAN Standard	IEEE 802.11a/n/ac, Wi-Fi compliant	
Frequency Range	4.900 GHz ~ 5.845 GHz (5.0 GHz ISM Band)	
Number of Channels	5.0GHz：Please see the table1	
Modulation	802.11a/n : 64-QAM,16-QAM, QPSK, BPSK 802.11ac : 256-QAM, 64-QAM,16-QAM, QPSK, BPSK	
Test Items	**Typical Value**	**EVM**
Output Power	802.11a /11Mbps : 15dBm ± 2 dB	EVM ≤ -10dB
	802.11n /MCS7(HT20) : 14dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7(HT40) : 14dBm ± 2 dB	EVM ≤ -28dB
	802.11ac/MCS8(VHT20) : 11 dBm±2 dB	EVM ≤ -30dB
	802.11ac/MCS9(VHT40) : 11 dBm±2 dB	EVM ≤ -32dB
	802.11ac/MCS9(VHT80) : 11 dBm±2 dB	EVM ≤ -32dB
Spectrum Mask	Meet with IEEE standard	
Receive Sensitivity (11a,20MHz) @8% PER	- 54Mbps PER @ -71 dBm	≤-65
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=7 PER @ -68 dBm	≤-64
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=7, PER @ -66 dBm	≤-61
Receive Sensitivity (11ac,20MHz)@10% PER	- MCS=8 PER @ -64 dBm	≤-59
Receive Sensitivity (11ac,40MHz) @10% PER	- MCS=9 PER @ -58 dBm	≤-54
Receive Sensitivity (11ac,80MHz) @10% PER	- MCS=9 PER @ -55 dBm	≤-51

4.3 Bluetooth Specification

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V5.0		
Host Interface	UART		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels for BDR+EDR 40 channels for BLE		
Modulation	GFSK, π/4-DQPSK, 8-DPSK		
RF Specification			
	Min(dBm)	**Typical**(dBm)	**Max**(dBm)
BDR Output Power		8	
BLE Output Power		8	
	Min	**Typical**	**IEEE**
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86	-70
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86	-70
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80	-70
Sensitive @PER=30.8% for BLE		-90	-70
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

5. ID setting information

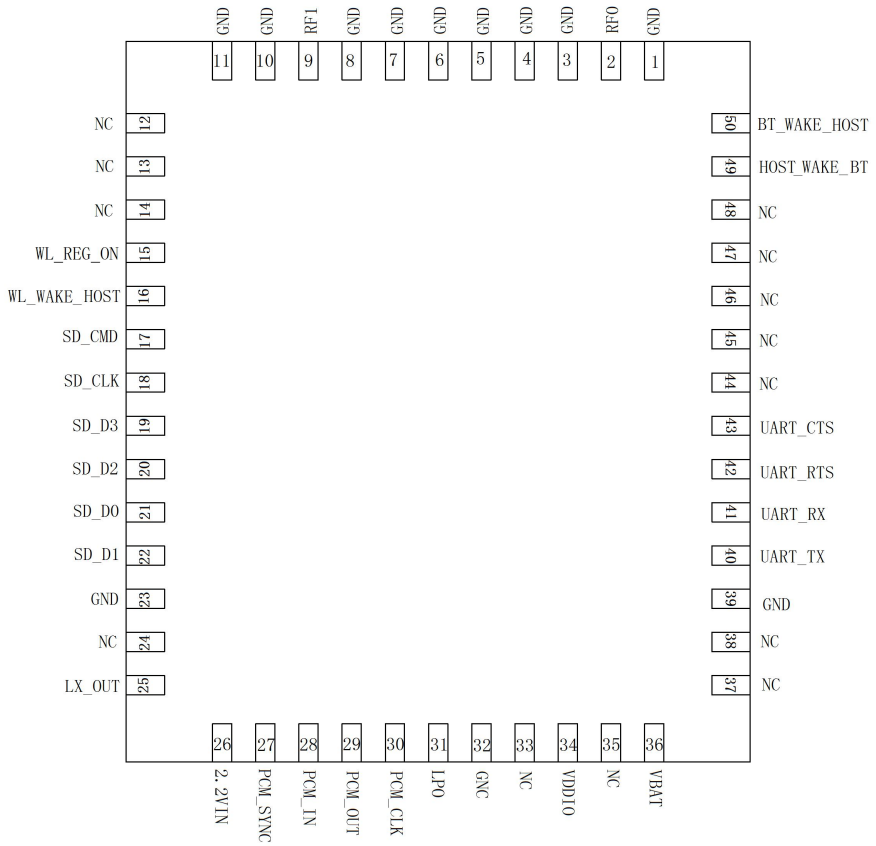
WI-FI

Vendor ID	0x02DF
Product ID	0x9141

6. Pin Definition

6.1 Pin Outline

< TOP VIEW >



6.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND		Ground connections	
2	RF0		WIFI_RF0	
3~8	GND		Ground connections	
9	RF1		WIFI_RF1/BT_RF	
10	GND		Ground connections	

11	GND		Ground connections	
12~14	NC		Floating (NC)	
15	WL_REG_ON	I	Full Power-Down When the host reboot, this pin should power down (active low)	VDDIO
16	WL_WAKE_HOST	O	WLAN to wake up HOST	VDDIO
17	SD_CMD	I/O	SDIO command line	VDDIO
18	SD_CLK	I/O	SDIO clock line	VDDIO
19	SD_D3	I/O	SDIO data line 3	VDDIO
20	SD_D2	I/O	SDIO data line 2	VDDIO
21	SD_D0	I/O	SDIO data line 0	VDDIO
22	SD_D1	I/O	SDIO data line 1	VDDIO
23	GND		Ground connections	VDDIO
24	NC		Floating (NC)	
25	LX_OUT	O	Need to connect a Power Inductor and then connect to pin26 (2.2V)	VDDIO
26	2.2VIN	I	DCDC_IN (2.2V)	
27	PCM_SYNC	I/O	PCM Sync	
28	PCM_IN	I/O	PCM Input	
29	PCM_OUT	I/O	PCM Output	
30	PCM_CLK	I/O	PCM Clock	
31	LPO	I	Crystals of up to 32.768 K	
32	GND		Ground connections	
33	NC		Floating (NC)	
34	VDDIO		Only control the Voltage of SDIO, Can be 1.8V or 3.3V	
35	NC		Floating (NC)	
36	VBAT		VDD3.3V	
37	NC		Floating (NC)	
38	NC		Floating (NC)	
39	GND		Ground connections	
40	UART_Tx		UART_Tx	
41	UART_Rx		UART_Rx	
42	UART_RTS		UART_RTS	
43	UART_CTS		UART_CTS	
44	NC		Floating (NC)	
45	NC		Floating (NC)	

46	NC		Floating (NC)	
47	NC		Floating (NC)	
48	NC		Floating (NC)	
49	HOST_WAKE_BT	I	Host device to wake up Bluetooth	
50	BT_WAKE_HOST	O	Bluetooth device to wake up host	

P:POWER I:INPUT O:OUTPUT VDDIO:3.3V

7. Electrical Specifications

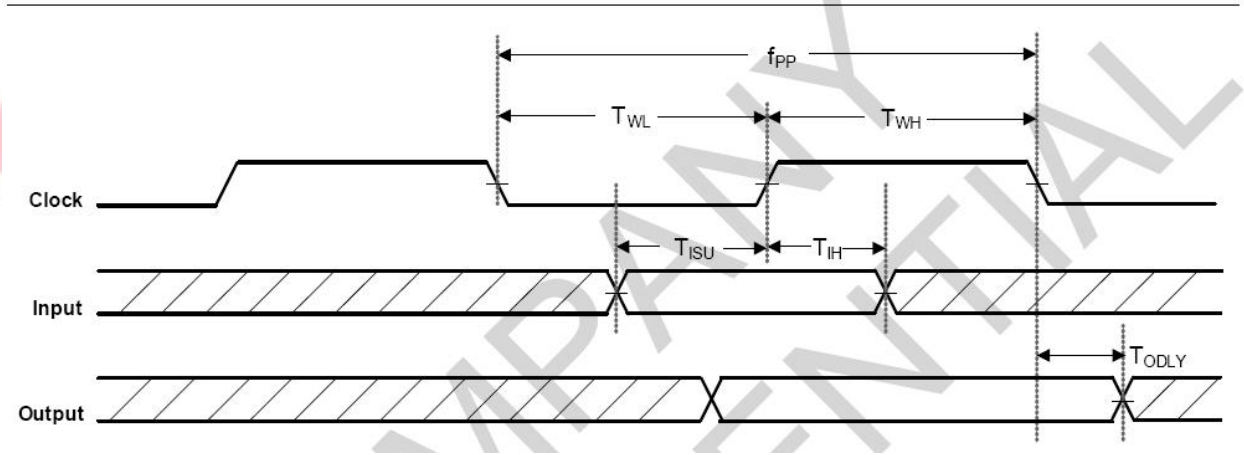
7.1 Host Interface Specifications

7.1.1 SDIO Specifications

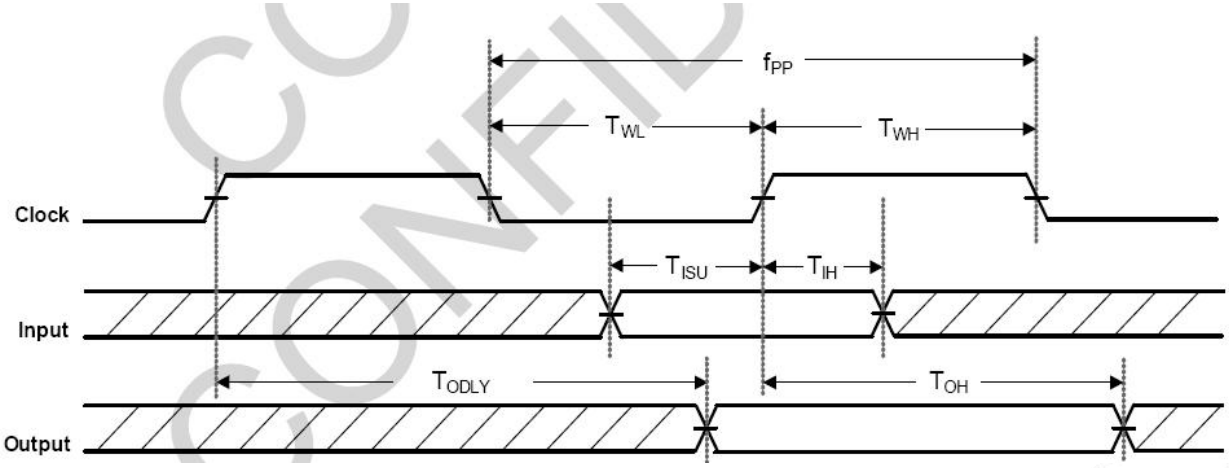
The SDIO host interface pins are powered from the VIO_SD voltage supply

7.1.2 Default Speed, High-Speed Modes

SDIO Protocol Timing Diagram—Default Speed Mode (3.3V)



SDIO Protocol Timing Diagram—High-Speed Mode (3.3V)



SDIO Timing Data—Default Speed, High-Speed Modes (3.3V)1, 2

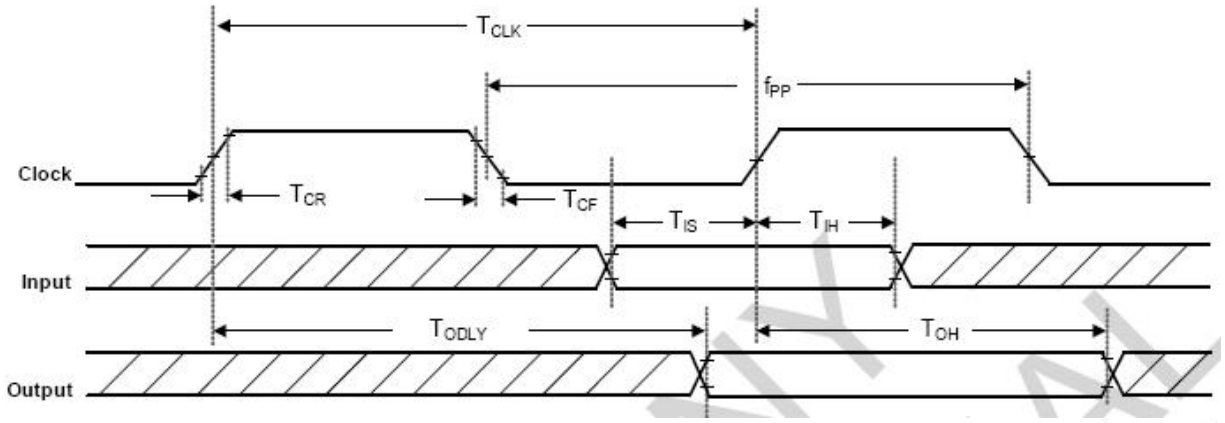
NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	Normal	0	--	25	MHz
		High-speed	0	--	50	MHz
T_{WL}	Clock low time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
T_{WH}	Clock high time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
T_{ISU}	Input setup time	Normal	5	--	--	ns
		High-speed	6	--	--	ns
T_{IH}	Input hold time	Normal	5	--	--	ns
		High-speed	2	--	--	ns
T_{ODLY}	Output delay time	Normal	--	--	14	ns
	CL ≤ 40 pF (1 card)	High-speed	--	--	14	ns
T_{OH}	Output hold time	High-speed	2.5	--	--	ns

1. For SDIO 2.0 running at 50 MHz clock frequency, only 1.8V is supported.
2. For SDIO 2.0 running at 25 MHz clock frequency, 1.8V or 3.3V is supported.

7.1.3 SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

SDIO Protocol Timing Diagram—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)



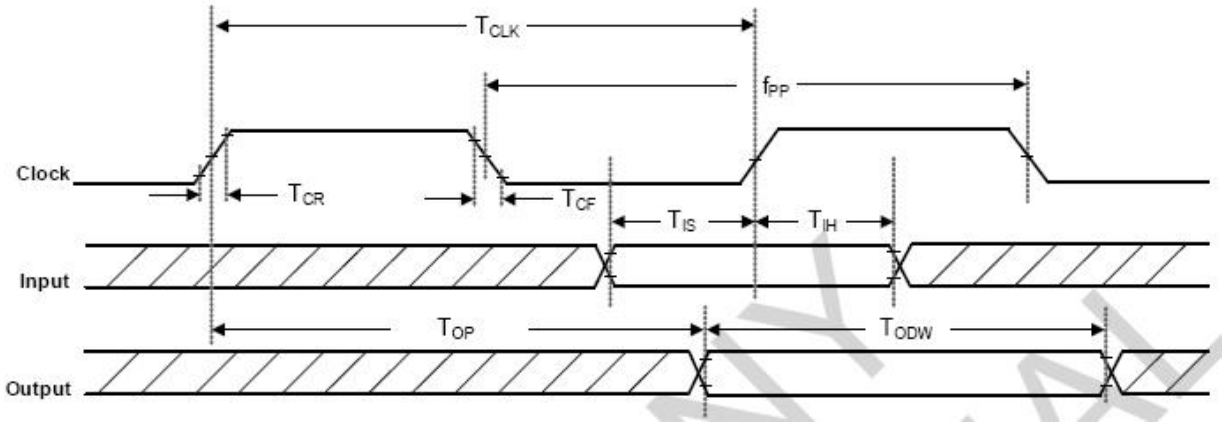
SDIO Timing Data——SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	--	--	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time C_L ≤ 30 pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	--	--	ns

7.1.4 SDR104 Mode (208 MHz) (1.8V)

SDIO Protocol Timing Diagram—SDR104 Mode (208 MHz)



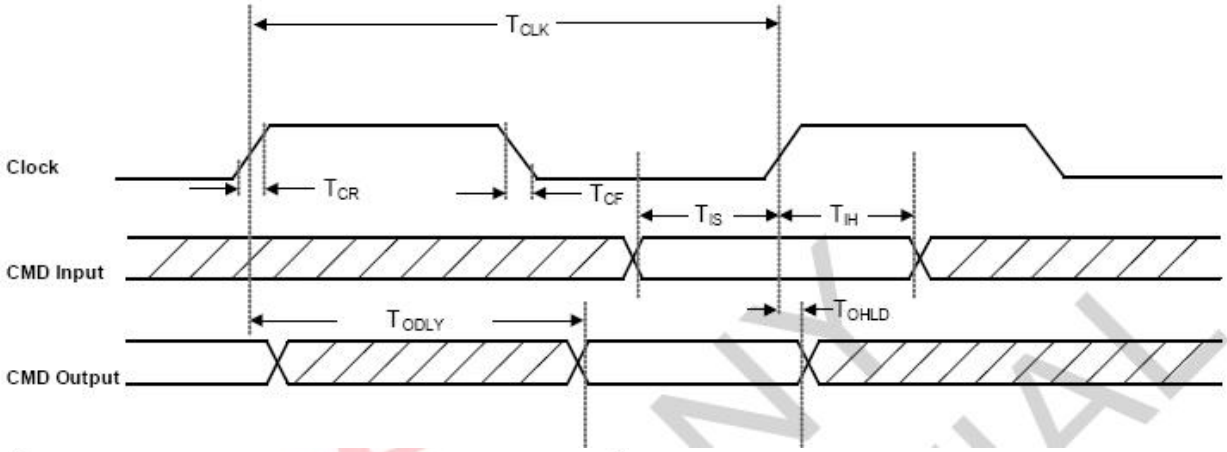
SDIO Timing Data—SDR104 Mode (208 MHz)

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

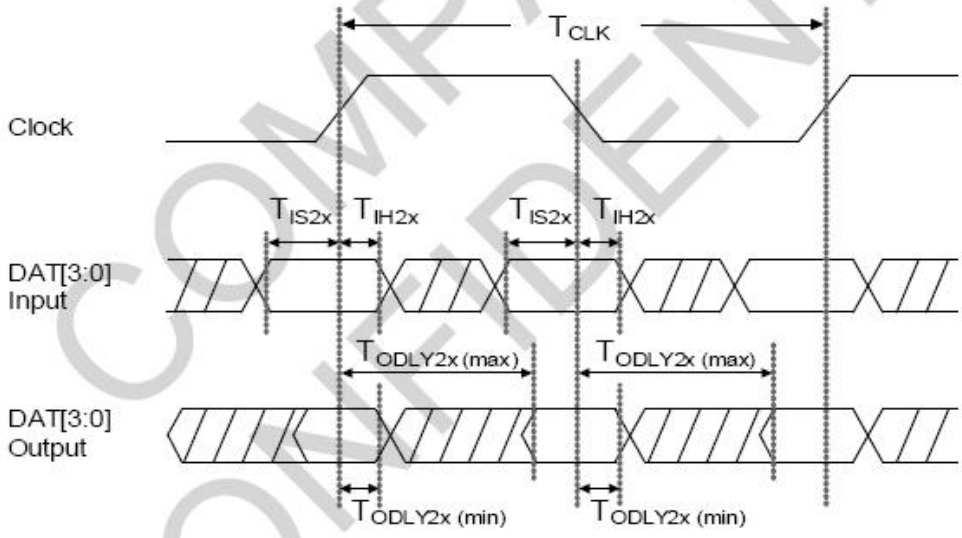
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR104	0	--	208	MHz
T_{IS}	Input setup time	SDR104	1.4	--	--	ns
T_{IH}	Input hold time	SDR104	0.8	--	--	ns
T_{CLK}	Clock time	SDR104	4.8	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	--	--	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	--	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	--	--	ns

7.1.5 DDR50 Mode (50 MHz) (1.8V)

SDIO CMD Timing Diagram—DDR50 Mode (50 MHz)



SDIO DAT[3:0] Timing Diagram—DDR50 Mode1 (50 MHz)



1. In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

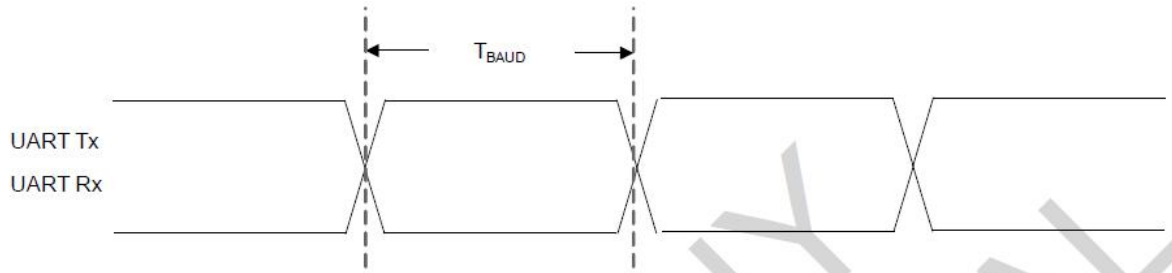
SDIO Timing Data—DDR50 Mode (50 MHz)

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR50	--	--	0.2*T_{CLK}	ns
Clock Duty	--	DDR50	45	--	55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6	--	--	ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	--	--	ns
CMD Output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50	--	--	13.7	ns
T_{OHLD}	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	--	--	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	3	--	--	ns
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	--	--	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x\ (max)}$	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50	--	--	7.0	ns
$T_{ODLY2x\ (min)}$	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	--	--	ns

7.2 High-Speed UART Specifications

7.2.1 UART Timing Diagram



UART Timing Data1

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{BAUD}	Baud rate	40 MHz input clock	250	--	--	ns

1. The acceptable deviation from the UART Rx target baud rate is ±3%.

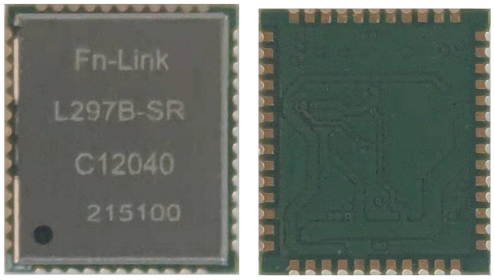
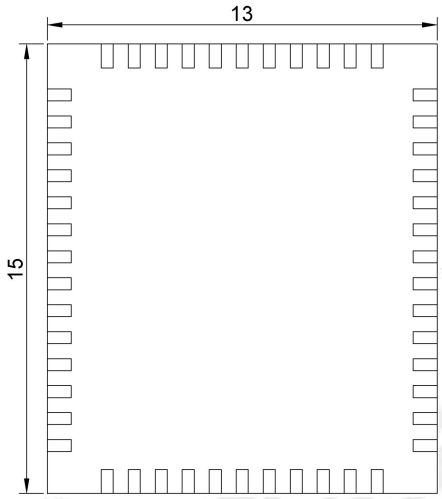
7.2.2 UART Baud Rates Supported

***Note:Default 115200**

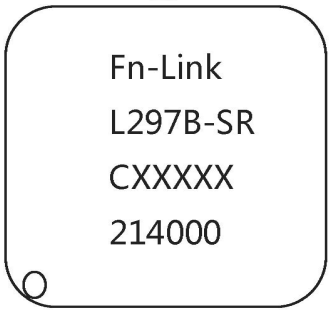
Baud Rate				
1200	38400	460800	1500000	3000000
2400	57600	500000	1843200	3250000
4800	76800	921600	2000000	3692300
9600	115200	1000000	2100000	4000000
19200	230400	1382400	2764800	--

8. Size reference

8.1 Module Picture

<table>
<tr><td>L x W : 13 x 15 (+0.3/-0.1) mm
 
</td><td> 
</td></tr>
<tr><td>H: 2.3 (±0.2) mm</td><td> 
</td></tr>
<tr><td>Weight</td><td>0.81</td></tr>
</table>

8.2 Marking Description



Brand name

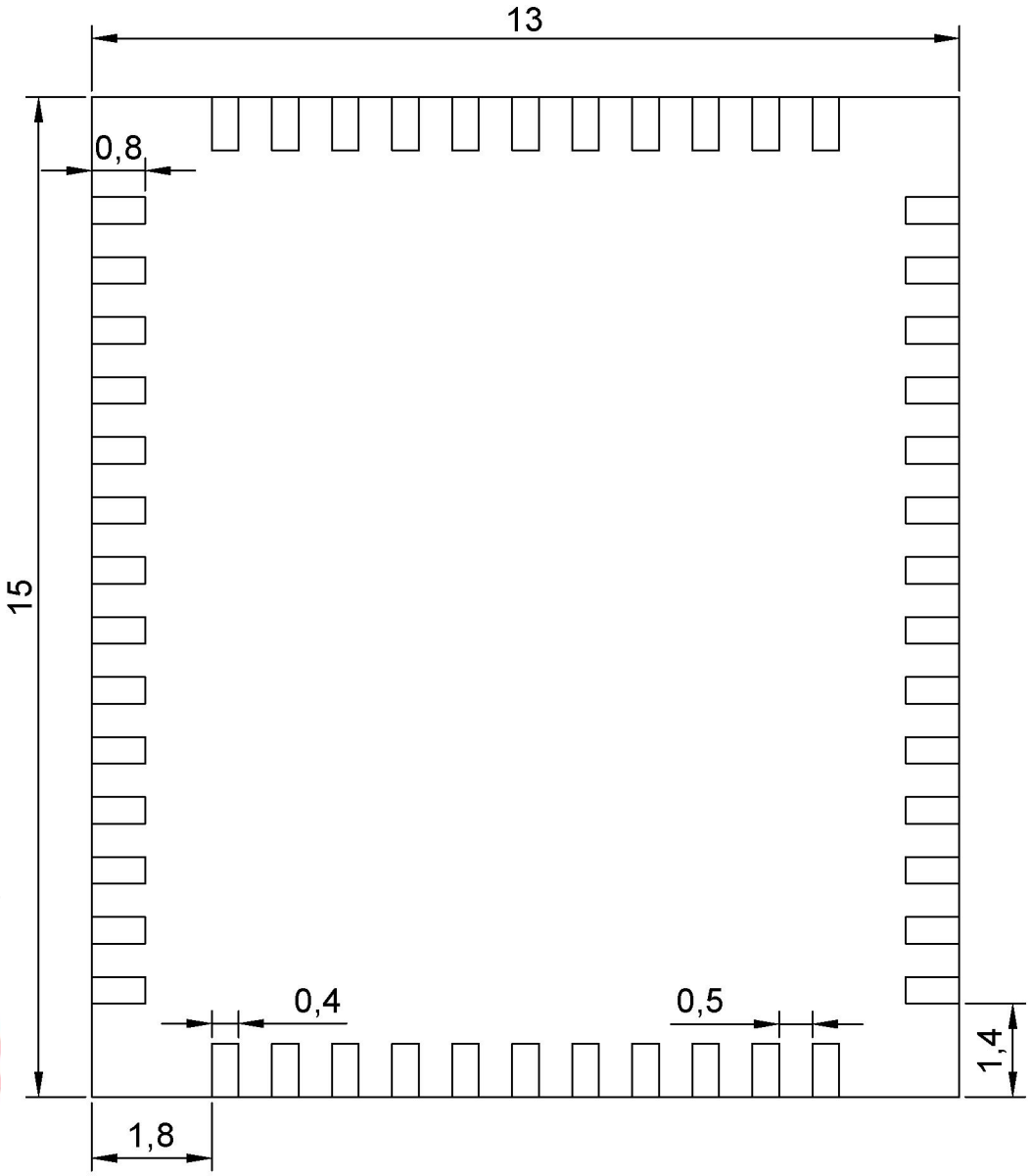
Model name

Lot code

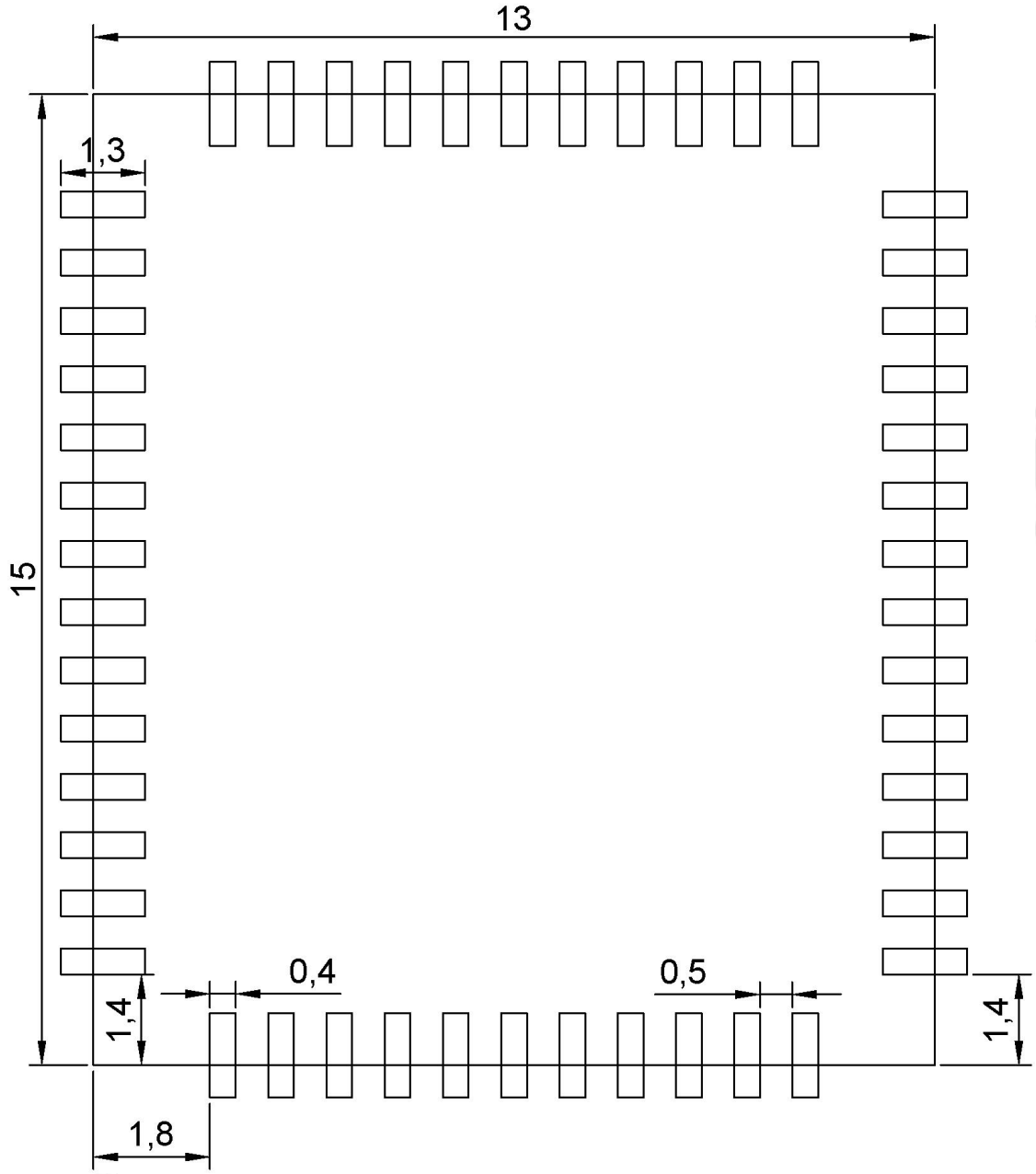
Date code

8.3 Physical Dimensions

<TOP View>



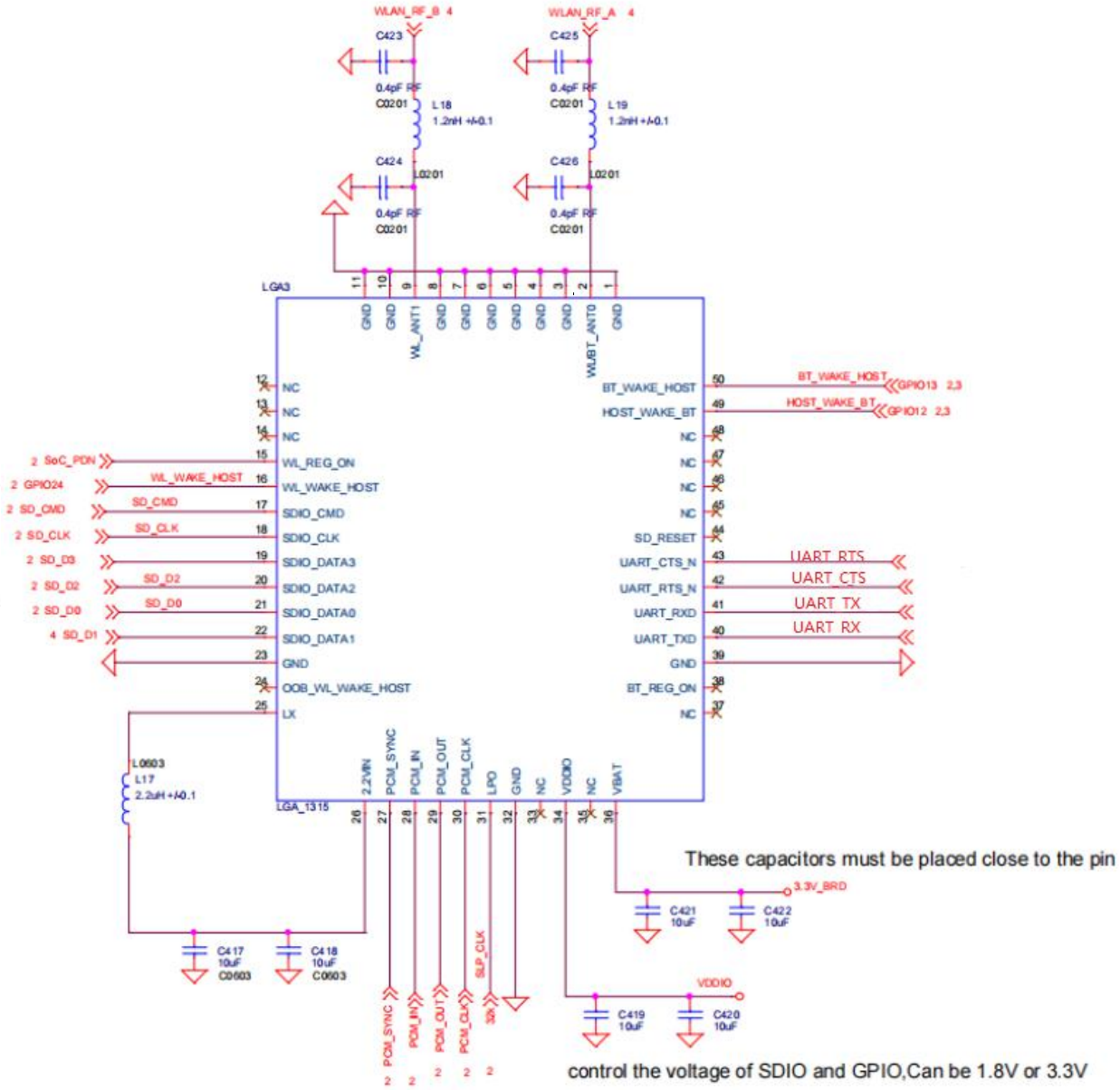
8.4 Layout Recommendation



9. The Key Material List

Chipset	NXP 88W8997	NXP
PCB	L297B-SR 深绿色,6L,FR4,13x15x0.8mm	XY-PCB,KX-PCB,SL-PCB,Sunlord
Crystal	2520 40MHz 12pF 10ppm	TST,HOSONIC,TKD,ECEC,JWT
Shielding	L297B-SR Shielding	信太,精力通

10. Reference Design



Note:1、L17 recommended specifications, 2016 2.2uH ,±20%，DCR＜0.17ohm，Isat≥1.9A，Irms≥1.45A，

The recommended P/N: WPN201610H2R（顺络）；CKCSA201610-2.2uH/M（岑科）

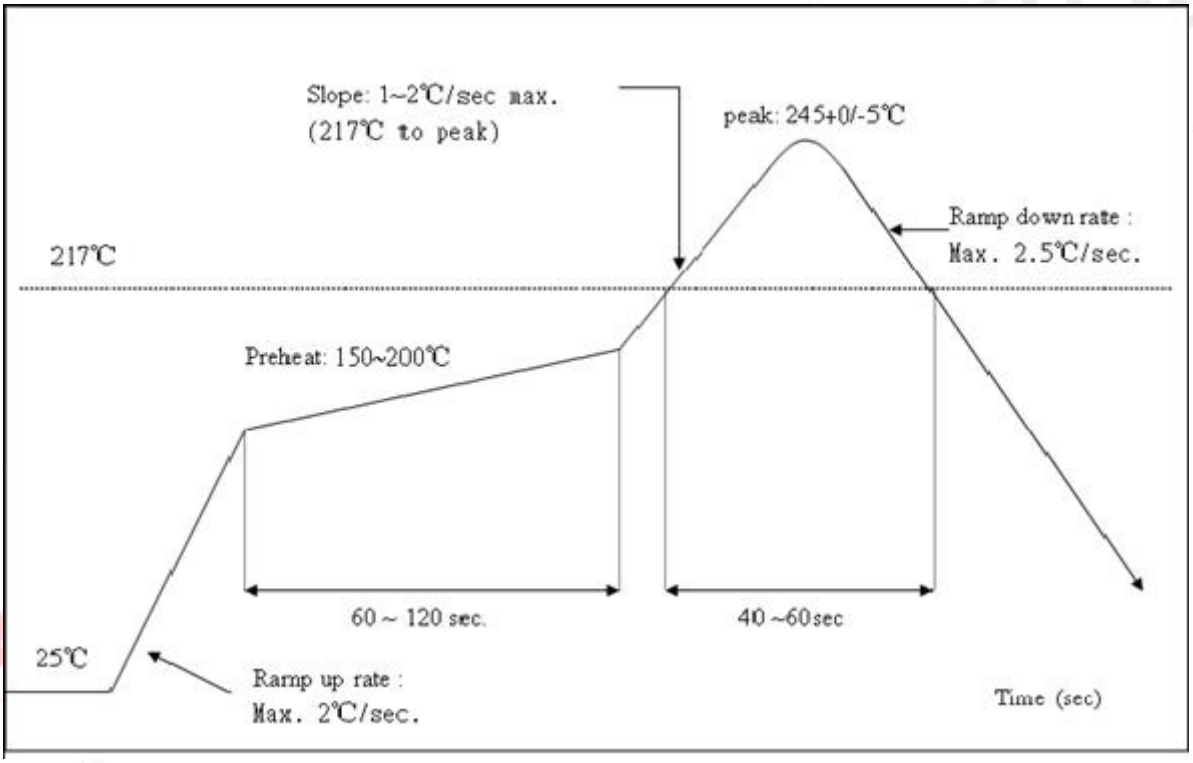
2、Full power dwon function must turn off the VBAT&VDDIO power supply from mainboard side。

11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

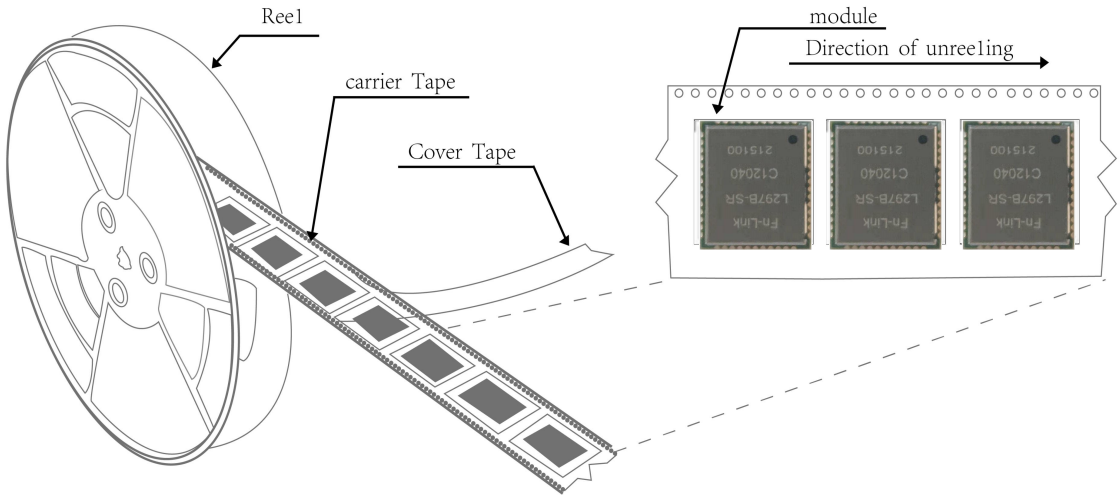
Number of Times : ≤2 times



12. Package

12.1 Reel

A roll of 1500pcs



12.2 Packaging Detail

the take-up package

Using self-adhesive tape

Size of black tape: 24mm*32.6m the cover tape :21.3mm*32.6m

Color of plastic disc: blue

NY bag size:460mm*385mm size ： 350*350*35mm

The packing case size:350*210*370mmg

13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more