

PRODUCT SPECIFICATIONS

P103N-U

LTE Standard Module Datasheet

Version: V1.0



P103N-U Module Datasheet

| Ordering Information | Part NO. | Description |
|----------------------|---------------|--|
| | FGP103NUXX-00 | ASR1603, LTE-FDD B1/B3/B5/B8, LTE-TDD B34/B38/B39/B40/B41, 3.8V, 22.9x21.9x2.4mm, with shielding |

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

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1. General Description

1.1 Introduction

P103N-U is a highly integrated LTE CAT1 module which supports both LTE-FDD and LTE TDD bands. It features application processing subsystem, communication subsystem, audio CODEC, and SoC embedded pSRAM. Both MCU and AP subsystem are able to run RTOS and user applications.

This compact module is a perfect choice for varies M2M application, such as security system, routers, wireless POS, PDA.

1.2 Description

| | |
|--------------------------------|--|
| Model Name | P103N-U |
| Product Description | Support LTE CAT1 applications |
| Dimension | L x W x H: 22.9 x 21.9 x2.4 mm |
| Interface | LTE, USB2.0, UART, PCM, (U)SIM, Audio, ADC, GPIO |
| OS supported | Android /Linux/ Windows |
| Operating temperature | -35°C to 75°C |
| Extended operating temperature | -40°C to 85°C |
| Storage temperature | -40°C to 90°C |

2. Features

SoC

- ASR1603E highly cost-efficient System on Chip
- Application Processor ARM Cortex-R5 up to 832MHz clock
- Embedded 16MB pSRAM and 16MB QSPI flash

Modem

- FDD/TDD LTE CAT1
- FDD B1/B3/B5/B8
- TDD B34/B38/B39/B40/B41

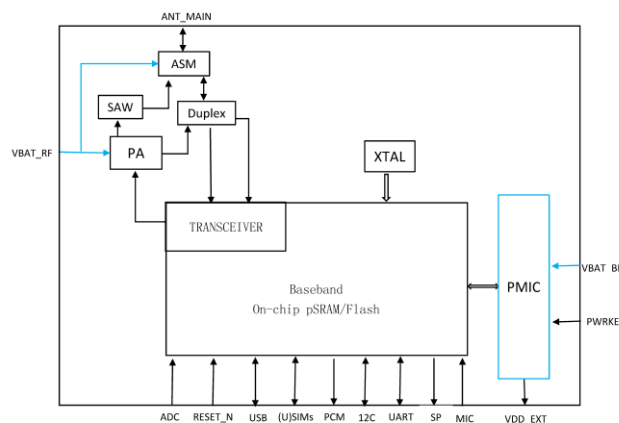
Audio CODEC

- Integrated High quality audio CODEC and audio front-end
- Single MIC input
- Mono differential RCV output
- Noise suppression and echo cancellation

Peripheral interfaces

- 1 x USB2.0 Device
- 2 x UART interface
- 1 x PCM master for external audio CODEC
- 1 x I2C
- 1 x 12-bit ADC

3. Block Diagram



4. General Specification

4.1 RF Transmit Specification

| Frequency band | Max. TX power | Min TX power |
|-----------------------------|---------------|--------------|
| LTE-FDD B1/B3/B5/B8 | 23 ±2 dBm | < -39 dBm |
| LTE-TDD B34/B38/B39/B40/B41 | 23 ±2 dBm | < -39 dBm |

Note: The RF specification will be updated in future version.

4.2 RF Receive Sensitivity

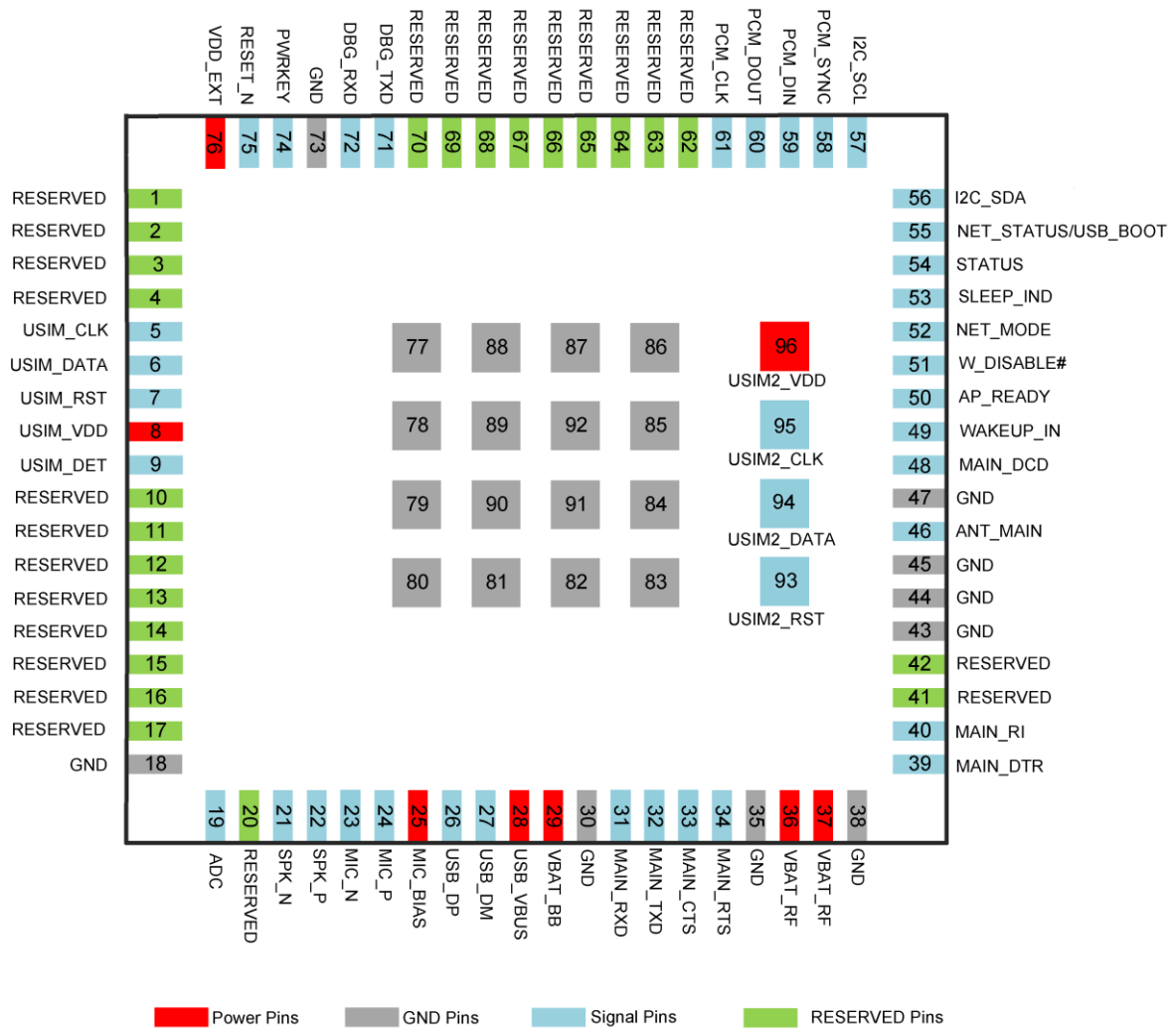
| Frequency band | RX Sensitivity | | | 3GPP Standard |
|----------------------|----------------|-----|---------|----------------|
| | PRX | DRX | PRX+DRX | 3GPP (PRX+DRX) |
| LTE-FDD B1 (10 MHz) | -98.5 dBm | N/A | N/A | -96.3 dBm |
| LTE-FDD B3 (10 MHz) | -98.0 dBm | N/A | N/A | -93.3 dBm |
| LTE-FDD B5 (10 MHz) | -99.5 dBm | N/A | N/A | -94.3 dBm |
| LTE-FDD B8 (10 MHz) | -99.0 dBm | N/A | N/A | -93.3 dBm |
| LTE-TDD B34 (10 MHz) | -99.0dBm | N/A | N/A | -96.3 dBm |
| LTE-TDD B38 (10 MHz) | -98.5dBm | N/A | N/A | -96.3 dBm |
| LTE-TDD B39 (10 MHz) | -99.0dBm | N/A | N/A | -96.3 dBm |
| LTE-TDD B40 (10 MHz) | -97.5dBm | N/A | N/A | -96.3 dBm |
| LTE-TDD B41 (10 MHz) | -97.5dBm | N/A | N/A | -94.3 dBm |

Note: The RF specification will be updated in future version.

5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



5.2 Pin Definition details

| NO. | Name | Type | Description | Voltage |
|-------|-----------|------|--|-------------|
| 1-4 | RESERVED | | Floating | |
| 5 | USIM_CLK | DO | (U)SIM card clock signal | |
| 6 | USIM_DATA | DIO | (U)SIM card data | |
| 7 | USIM_RST | DO | (U)SIM card reset | |
| 8 | USIM_VDD | PO | (U)SIM card power supply | 1.8 / 3.0 V |
| 9 | USIM_DET | DI | (U)SIM card insertion detection, NC if not use | |
| 10-17 | RESERVED | | Floating | |
| 18 | GND | | Ground connections | |
| 19 | ADC | AI | Analog to digital converter input, NC if not use | 0~1.3V |
| 20 | RESERVED | | Floating | |
| 21 | SPK_N | AO | Audio differential output - , NC if not use | |
| 22 | SPK_P | AO | Audio differential output + , NC if not use | |
| 23 | MIC_N | AI | Audio differential input - , NC if not use | |
| 24 | MIC_P | AI | Audio differential input + , NC if not use | |
| 25 | MIC_BIAS | PO | Bias voltage for MIC | |
| 26 | USB_DP | DIO | USB data+ | |
| 27 | USB_DM | DIO | USB data- | |
| 28 | USB_VBUS | AI | USB detection, NC if not use | |
| 29 | VBAT_BB | PI | Power supply of base-band | |
| 30 | GND | | Ground connections | |
| 31 | MAIN_RXD | DI | Main UART input, NC if not use | |
| 32 | MAIN_TXD | DO | Main UART output, NC if not use | |
| 33 | MAIN_CTS | DO | Main UART Clear To Send, NC if not use | |
| 34 | MAIN_RTS | DI | Main UART Request To Send, NC if not use | |
| 35 | GND | | Ground connections | |
| 36 | VBAT_RF | PI | Power supply of RF | |
| 37 | VBAT_RF | PI | Power supply of RF | |
| 38 | GND | | Ground connections | |
| 39 | MAIN_DTR | DI | Main UART Data Terminal Ready, NC if not use | |
| 40 | MAIN_RI | DO | Main UART Ring Indicator, NC if not use | |
| 41 | RESERVED | | Floating | |
| 42 | RESERVED | | Floating | |
| 43-45 | GND | | Ground connections | |
| 46 | ANT_MAIN | AIO | Main antenna interface | |
| 47 | GND | | Ground connections | |

| | | | | |
|-------|----------------------------|-----|--|-------------|
| 48 | MAIN_DCD | DO | Main UART Data Carrier Detect, NC if not use | |
| 49 | WAKEUP_IN | DI | Wake up signal input for module, NC if not use | |
| 50 | AP_READY | DI | HOST sleep mode detection, NC if not use | |
| 51 | W_DISABLE# | DI | Flight mode control, NC if not use | |
| 52 | NET_MODE | DO | Indicator of network standard, NC if not use | |
| 53 | SLEEP_IND | DO | Indicator of sleep mode, NC if not use. DO NOT pull low before module totally boot up. | |
| 54 | STATUS | DO | Indicator of working status, NC if not use | |
| 55 | NET_STATUS/USB_BOOT | DO | Network status ^{Note1} , Multiplexing used as emergency download mode control (active low). | |
| 56 | I2C_SDA | OD | I2C serial data, for external codec, NC if not use | |
| 57 | I2C_SCL | OD | I2C serial clock, for external codec, NC if not use | |
| 58 | PCM_SYNC | DO | PCM frame synchronization, NC if not use | |
| 59 | PCM_DIN | DI | PCM data input, NC if not use | |
| 60 | PCM_DOUT | DO | PCM data output, NC if not use | |
| 61 | PCM_CLK | DO | PCM clock, NC if not use | |
| 62-70 | RESERVED | | Floating | |
| 71 | DBG_TXD | DO | Debug UART output, NC if not use | |
| 72 | DBG_RXD | DI | Debug UART input, NC if not use | |
| 73 | GND | | Ground connections | |
| 74 | PWRKEY | DI | Module turn on/off | |
| 75 | RESET_N | DI | Module reset, NC if not use | |
| 76 | VDD_EXT | PO | Power for external 1.8V PU, NC if not use | 1.8V |
| 77-92 | GND | | Ground connections | |
| 93 | USIM2_RST ^{Note2} | DO | (U)SIM2 card reset | |
| 94 | USIM2_DATA | DIO | (U)SIM2 card data | |
| 95 | USIM2_CLK | DO | (U)SIM2 card clock signal | |
| 96 | USIM2_VDD | PO | (U)SIM2 card power supply | 1.8 / 3.0 V |

Note1: Please be noted that module will access emergency download mode if this pin is pulled to low level when power up. In download mode, user can upgrade FW with USB interface. If this pin is high when module power up, it will be configured as network status indicator, please use MOSFET circuit instead of BJT for LED control. For more details, please check reference design.

Note2: (U)SIM2 is not available for now. Please contact Fn-Link for further information.

6. Electrical Specifications

6.1 Absolute Maximum Ratings

| Symbol | Min. | Max. | unit |
|--------------------|------|------|------|
| VBAT_RF | -0.3 | 6 | V |
| VBAT_BB | -0.3 | 6 | V |
| USB_VBUS | -0.3 | 5.5 | V |
| Current of VBAT_BB | 0 | 0.5 | A |
| Current of VBAT_RF | 0 | 1.5 | A |
| VIO | -0.3 | 2.3 | V |

6.2 Operating Conditions

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|----------|---------------------------|---|---------|------|---------------------|------|
| VBAT | VBAT_BB and VBAT_RF | Input voltage must be within this range | 3.4 | 3.8 | 4.5 | V |
| IVBAT | Peak current | At max. transmitting power | - | 1.5 | 2.0 | A |
| USB_VBUS | USB power supply | - | 3.0 | 5.0 | 5.25 | V |
| VOH | High level output voltage | High = -500uA | 0.8*VDD | | VDD ^{Note} | V |
| VOL | Low level output voltage | Low = 500uA | 0 | | 0.2*VDD | |
| VIH | High level input voltage | | 0.7*VDD | | VDD+0.3 | V |
| VIL | Low level input voltage | | -0.3 | | 0.48 | V |

Note: VDD = 1.8V.

6.3 Operating and storage temperature

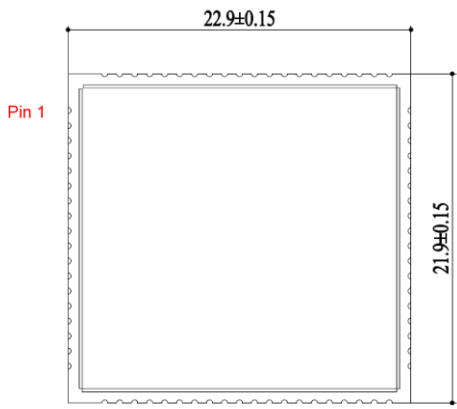
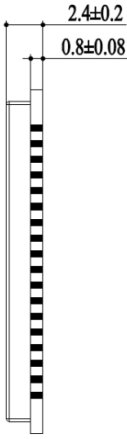
| | |
|---|---------------|
| Operating temperature ^{Note1} | -35°C to 75°C |
| Extended operating temperature ^{Note2} | -40°C to 85°C |
| Storage temperature | -40°C to 90°C |

Note1: When the module operates within this temperature range, the performance can meet 3GPP standard.

Note2: When the module operates within this temperature range, functions will be OK and no permanent damage will occur. A few parameters such as RF output power may exceed the range of 3GPP standards. When the temperature returns to the normal operating temperature range, module can still meet 3GPP standards.

7. Size Reference

7.1 Module Picture

| | |
|--|--|
|  <p>Top view diagram of the module showing dimensions: width 22.9 ± 0.15, height 21.9 ± 0.15, and Pin 1 location.</p> |  <p>Side view diagram of the module showing dimensions: thickness 2.4 ± 0.2 and another dimension 0.8 ± 0.08.</p> |
| Weight | TBD |

8. The Key Material List

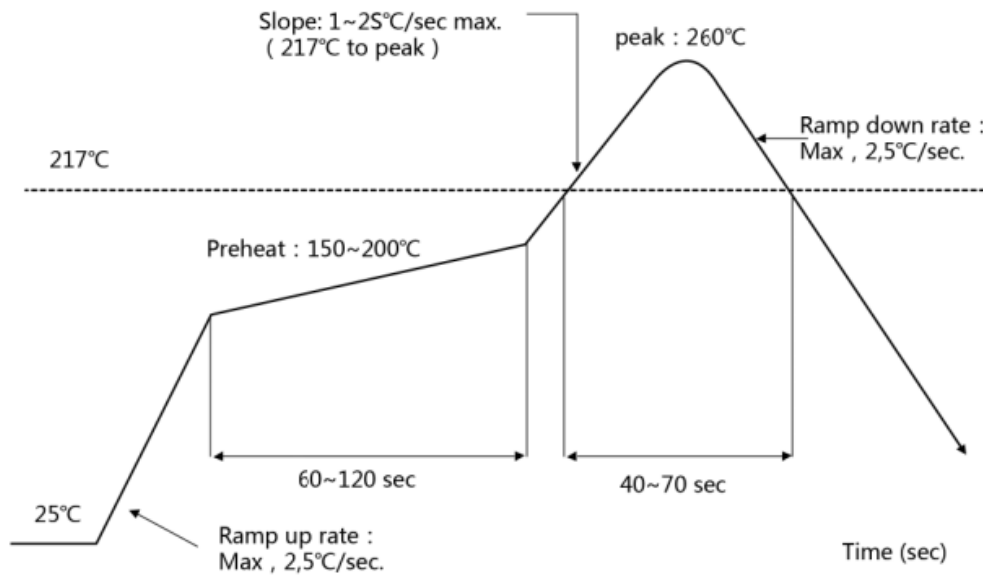
| | | |
|-----------|--|--------------------------------------|
| Chipset | ASR1603S, LTE CAT1, BGA203, 7.4x7.4mm | ASR |
| PCB | P103N-U-V1.0, HDI 6L, Tg150, 21.9X22.9X0.8mm | Brain-power, KX-PCB, SL-PCB, Sunlord |
| Crystal | 2016 26MHz 9pF 8ppm | TST, HOSONIC, TKD, ECEC, JWT |
| Inductor | 2016 1.0uH , ±20% , >2A | Sunlord, Cenke, Ceaiya, Microgate |
| Shielding | P103N-U-V1.0 shielding, 21.5x20.5x1.4mm, T=0.2mm | Suntech, JLT |

9. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

Number of Times : ≤2 times



10. RoHS Compliance

All hardware components are fully compliant with EU RoHS directive.

11. Moisture Sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
- b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
- c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
- d) Baking is required if conditions b) or c) are not respected
- e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more